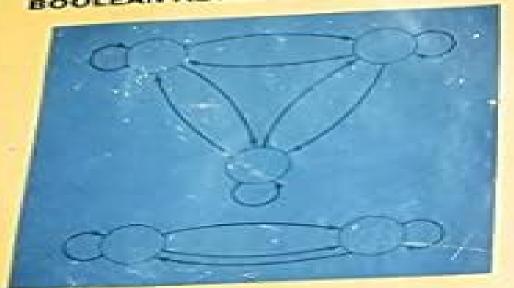
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Logic Synthesis and Verification Algorithms Gary D. Hachtel, Fabio Somenzi, 2005-12-17 Logic Synthesis and Verification Algorithms is a textbook designed for courses on VLSI Logic Synthesis and Verification Design Automation CAD and advanced level discrete mathematics It also serves as a basic reference work in design automation for both professionals and students Logic Synthesis and Verification Algorithms is about the theoretical underpinnings of VLSI Very Large Scale Integrated Circuits It combines and integrates modern developments in logic synthesis and formal verification with the more traditional matter of Switching and Finite Automata Theory The book also provides background material on Boolean algebra

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