The Electronic Design Interchange Format EDIF: Present and Future

Hilary J. Kahn
Dept. of Computer Science
University of Manchester
Oxford Road, Manchester, M13 9PL UK

Richard F. Goldman
Texas Instruments Inc
P.O. Box 655303
Dallas, TX, USA 75265

Abstract

This paper reviews the present status and current development of the Electronic Design Interchange Format, EDIF. After a review of the role EDIF has at present, some of the new ideas being developed for inclusion in the new release of EDIF (Version 2 1 0) are introduced.

1: Introduction

Work on the definition of the Electronic Design Interchange Format EDIF started in 1983 and the first balloted version of the EIA standard, EDIF Version 2 0 0, was published in 1987. It became an ANSI standard as well in 1988 [1]. At the time, EDIF offered a way forward for end users and developers alike. For the end user in particular, it gave hope that there really could be a choice of design tools for different design stages (say) by transferring design information between different CAE systems, and the route to silicon or manufacture in general would have choices because a neutral format for transfer was available.

The original enthusiasm for EDIF assumed that it would be feasible – both technically and commercially – for CAD vendors to implement conformant transfer software. The reality has turned out to be rather different in some respects. It is true that the EDIF format is not without flaws; however the format is considerably more powerful and applicable than much current CAD vendor software permits. There have nonetheless been failures to understand the format and somewhat liberal interpretations of its semantics.

Despite problems, EDIF is now the primary mechanism for transfer of connectivity and schematic data. However, real practical problems exist and are being tackled. In this paper some of the difficulties that have arisen are reviewed and some solutions are discussed. The paper also summarises some of the extensions that are to be available as the next release of EDIF.

2: EDIF Version 2 0 0: Technical Status

EDIF Version 2 0 0 is intended primarily as a mechanism for the transfer of design information between CAD systems or from CAD systems, through to manufacture. At the time when it was first developed, the main interest in the format was to be found among silicon houses and CAD vendors whose products supported design to silicon. It followed therefore that the capabilities of EDIF Version 2 0 0 should have been focused on meeting the needs of transfers of interest to ASIC designers.

EDIF offers a very structured representation of design data. The information is gathered into a set of libraries, which will typically hold information which is related by use (e.g. a library of schematic symbols) or by technology. Within a library the information is structured into a set of cells which are the main unit of design. Within a cell, the information is further structured into a set of views. The allowable types of view relate closely to the stages of the design process and hence directly to the points in the design process where design transfer may be expressed. In EDIF Version 2 0 0, the main design related views are:

- NETLIST. This captures connectivity information together with aspects of timing specification.
- SCHEMATIC. This allows schematic symbols to be defined and provides for the description of multi-page schematic diagrams. The underlying connectivity represented by the schematic may also be captured. Again, timing information may be included.
- MASKLAYOUT. This captures the geometric layout of an IC together with the underlying connectivity.
- SYMBOLIC LAYOUT. This is intended to capture layout information and connectivity in terms of an abstract symbolic representation instead of mask level layout.
- LOGICMODEL. This type of view allows the behaviour of a cell to be described using an event driven modelling representation.
- PCBLAYOUT. This view does not have adequate capability in EDIF Version 2 0 0. It is intended to support the definition of printed circuit board geometry and the underlying connectivity it represents.

An important characteristic of the EDIF design representations is that they are all capable of capturing the details of design hierarchy. This means that an EDIF description can accurately capture the instance and definition hierarchies found in databases which support electronic CAD processes.

Edif Electronic Design Interchange Format Version 200

J Elliott

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   EDIF ,1990   **The Electronic Design Automation Handbook** Dirk Jansen,2010-02-23 When I attended college we studied vacuum tubes in our junior year At that time an average radio had ve vacuum tubes and better ones even seven Then transistors appeared in 1960s A good radio was judged to be one with more thententransistors Latergoodradioshad15 20transistors and after that everyone stopped counting transistors Today modern processors runing personal computers have over 10milliontransistorsandmoremillionswillbeaddedevery year The difference between 20 and 20M is in complexity methodology and business models Designs with 20 tr sistors are easily generated by design engineers without any tools whilst designs with 20M transistors can not be done by humans in reasonable time without the help of Prof Dr Gajski demonstrates the Y chart automation This difference in complexity introduced a paradigm shift which required sophisticated methods and tools and introduced design automation into design practice By the decomposition of the design process into many tasks and abstraction levels the methodology of designing chips or systems has also evolved Similarly the business model has changed from vertical integration in which one company did all the tasks from product speci cation to manufacturing to globally distributed client server production in which most of the design and manufacturing tasks are outsourced   Electronic Design Automation Frameworks Franz J. Rammig,Flavio Wagner,2013-04-17 Design frameworks have become an important infrastructure for building complex design systems Electronic Design Automation Frameworks presents a state of the art review of the latest research results covering this topic results which are also of value for other design frameworks The book contains the selected proceedings of the Fourth International Working Conference on Electronic Design Frameworks organized by the International Federation for Information Processing and held in Gramado Brazil in November 1994   VHDL Modeling for Digital Design Synthesis Yu-Chin Hsu,Kevin F. Tsai,Jessie T. Liu,Eric S. Lin,2012-12-06 The purpose of this book is to introduce VHSIC Hardware Description Lan guage VHDL and its use for synthesis VHDL is a hardware description language which provides a means of specifying a digital system over different levels of abstraction It supports behavior specification during the early stages of a design process and structural specification during the later implementation stages VHDL was originally introduced as a hardware description language that per mitted the simulation of digital designs It is now increasingly used for design specifications that are given as the input to synthesis tools which translate the specifications into netlists from which the physical systems can be built One problem with this use of VHDL is that not all of its constructs are useful in synthesis The specification of delay in signal assignments does not have a clear meaning in synthesis where delays have already been determined by the im plementationtechnolo y VHDL has data structures such as files and pointers useful for simulation purposes but not for actual synthesis As a result synthe sis tools accept only subsets of VHDL This book tries to cover the synthesis aspect of VHDL while keeping the simulation specifics to a minimum This book is suitable for working professionals as well as for graduate or under graduate study Readers can view

this book as a way to get acquainted with VHDL and how it can be used in modeling of digital designs **Simulation Systems** George Zobrist,James V. Leonard,2000-04-17 Simulation Systems expolres a wide spectrum of topics including simulation software logic simulation query driven simulation multi computer simulation and manufacturing simulation Although such papers are presented in Journals and conference proceedings it is difficult to find a single source where the foremost papers are presented Contributio VLSI Design Environments George Zobrist,2000-04-17 VLSI Design Environments investigates design alternatives such as object oriented data modelling The difficulty of automating chip architecture designs is caused by the complexity of the problem The explosion of design decions make a heuristic approach necessary PLAYOUT aims at the solution of system problems based on hierarchy top down planning silicon complier presentations advances in encoding logic synthesis and a microarchitecre and logic optimization system PLAYOUT supports the physical design from entering the structure of digital systems to the generation of the mask The concept for autonomous tools with a clear interface to the network description and the simple interface to the graphics is presented This enables the designer to have a great influence on the configuration of the placement of the schematic diagram Substantial progress is being made in behavioural and logic synthesis both of which depend upon specifications **Cad Frameworks** Pieter van der Wolf,2012-12-06 Since the early 1980s CAD frameworks have received a great deal of attention both in the research community and in the commercial arena It is generally agreed that CAD framework technology promises much advanced CAD frameworks can turn collections of individual tools into effective and user friendly design environments But how can this promise be fulfilled CAD Frameworks Principles and Architecture describes the design and construction of CAD frameworks It presents principles for building integrated design environments and shows how a CAD framework can be based on these principles It derives the architecture of a CAD framework in a systematic way using well defined primitives for representation This architecture defines how the many different framework sub topics ranging from concurrency control to design flow management relate to each other and come together into an overall system The origin of this work is the research and developmentperformed in the context of the Nelsis CAD Framework which has been a working system for well over eight years gaining functionality while evolving from one release to the next The principles and concepts presented in this book have been field tested in the Nelsis CAD Framework CAD Frameworks Principles and Architecture is primarily intended for EDA professionals both in industry and in academia but is also valuable outside the domain of electronic design Many of the principles and concepts presented are also applicable to other design oriented application domains such as mechanical design or computer aided software engineering CASE It is thus a valuable reference for all those involved in computer aided design *Power Semiconductor Devices and Circuits* A.A. Jaecklin,2012-12-06 This symposium was the sCientific technical event of the centennial celebration of the Asea Brown Boveri Switzerland The purpose was to assess the present state of the art as well as shaping the basis for future progress in the area of power devices and related power

circuits The merger of Brown Boveri BBC with Asea to Asea Brown Boveri ABB three years ago gave new stimulus and enriched the technical substance of the symposium By 1991 100 years after the formation of BBC in Switzerland as a single company this organization has been decentralized forming 35 independent ABB companies One of them ABB Semiconductors Ltd directly deals with the power semiconductor business These significant changes reflect the changes in the market place increased competition and higher customer expectations have to be fulfilled In line with the core business activities of ABB and with the concept of sustainable development it is natural for ABB to be active in the area of power devices and circuits Increased awareness towards energy conservation is one of the main drives for these activities User friendliness is another drive integration of intelligent functions e g protection and or increased direct computer interfacing of the power circuits Therefore also the R D activities related to the subject of thIs symposium will in the future be characterized by an even stronger coupling with the market needs For the members of the R D Laboratories this means improved customer partnership beyond operational excellence **High-Performance Computing** Laurence T. Yang,Minyi Guo,2006-01-24 The state of the art of high performance computing Prominent researchers from around the world have gathered to present the state of the art techniques and innovations in high performance computing HPC including Programming models for parallel computing graph oriented programming GOP OpenMP the stages and transformation SAT approach the bulk synchronous parallel BSP model Message Passing Interface MPI and Cilk Architectural and system support featuring the code tiling compiler technique the MigThread application level migration and checkpointing package the new prefetching scheme of atomicity a new receiver makes right data conversion method and lessons learned from applying reconfigurable computing to HPC Scheduling and resource management issues with heterogeneous systems bus saturation effects on SMPs genetic algorithms for distributed computing and novel task scheduling algorithms Clusters and grid computing design requirements grid middleware distributed virtual machines data grid services and performance boosting techniques security issues and open issues Peer to peer computing P2P including the proposed search mechanism of hybrid periodical flooding HPF and routing protocols for improved routing performance Wireless and mobile computing featuring discussions of implementing the Gateway Location Register GLR concept in 3G cellular networks maximizing network longevity and comparisons of QoS aware scatternet scheduling algorithms High performance applications including partitioners running Bag of Tasks applications on grids using low cost clusters to meet high demand applications and advanced convergent architectures and protocols High Performance Computing Paradigm and Infrastructure is an invaluable compendium for engineers IT professionals and researchers and students of computer science and applied mathematics **Tool Integration and Design Environments** F. J. Rammig,1988 This volume is a documentation of a workshop which brought together active researchers in the field of CAD for hardware design The main features are as follows recent research results in the field of hardware design environments comparison of different approaches of tool integration evolution from isolated tools to integrated design

systems The book is divided into the following sections data management data models open systems integrated systems tool boxes language based systems and design management   Engineering Databases Jose L. Encarnacao,Peter C. Lockemann,2012-12-06 Automation is nothing new to industry It has a long tradition on the factory floor where its constant objective has been to increase the productivity of manufacturing processes Only with the advent of computers could the focus of automation widen to include administrative and information handling tasks More recently automation has been extended to the more intellectual tasks of production planning and control material and resource planning engineering design and quality control New challenges arise in the form of flexible manu facturing assembly automation and automated floor vehicles to name just a few The sheer complexity of the problems as well as the state of the art has led scientists and engineers to concentrate on issues that could easily be isolated For example it was much simpler to build CAD systems whose sole objective was to ease the task of drawing rather than to worry at the same time about how the design results could be interfaced with the manufacturing or assembly processes It was less problematic to gather statistics from quality control and to print reports than to react immediately to first hints of irregularities by inter facing with the designers or manufacturing control or even better by auto matically diagnosing the causes from the design and planning data A heav though perhaps unavoidable price must today be paid whenever one tries to assemble these isolated solutions into a larger integrated system   **Proceedings of the ... Custom Integrated Circuits Conference** ,1987   **Computer Aided Systems Theory - EUROCAST '91** Franz Pichler,Roberto Moreno Diaz,1992-04-08 This volume contains a selection of papers presented at the second European workshop EUROCAST 91 held in Krems Austria in April 1991 It gives an overview of the current state of Computer Aided Systems Theory research and its relation to CAD applications in the engineering fields CAST research requires the application of the most advanced information processing technology in software and hardware for the implementation of CAST method base systems Engineers in the field of information and control engineering have the opportunity in CAST to present the state ofthe art in modeling tools to computer scientists EUROCAST 91 proved that CAST research is still in an early state of development The papers in the volume are organized into sections on systems theory and CAST methodology modeling environments CAST method base systems and artificial vision and information and control systems   **SMC XII** ,1987   **Electro ... Conference Record** ,1989   *IEEE Proceedings of the Southeastcon* ,1992   *Evolvable Hardware* Martin A. Trefzer,Andy M. Tyrrell,2015-09-14 This book covers the basic theory practical details and advanced research of the implementation of evolutionary methods on physical substrates Most of the examples are from electronic engineering applications including transistor level design and system level implementation The authors present an overview of the successes achieved and the book will act as a point of reference for both academic and industrial researchers   **Computer Hardware Description Languages and Their Applications** Mario R. Barbacci,Cees-Jan Koomen,1987 The symposium on which this book is based has become established as the focal point for the meeting of experts in the field of

formal descriptions of hardware and their use in analysis and synthesis of digital systems The papers reflect the gradual shift from the original emphasis on the uses of language design to describe hardware toward more formal techniques for specification and verification *Economics of Design and Test for Electronic Circuits and Systems* M. Abadir,1992

Datenhaltung in VLSI-Entwurfssystemen Johannes Brauer,2013-12-01 Wesentliche Teile dieses Buches sind w hrend meiner T tigkeit als Hochschul assistent an der Universit t Gesamthochschule Siegen entstanden und bildeten die Grundlage f r die Erlangung der Venia legendi Ich m chte an dieser Stelle meinen Gutachtern Herrn Prof Dr Wojtkowiak und Herrn Prof Dr Wegner sowohl f r die Bereitschaft die Arbeit zu begutachten als auch f r die zahlrei chen Anregungen und Verbesserungsvorschl ge f r die Ver ffentlichung als Buch herzlich danken Letzteres gilt auch f r die Herren aus dem Herausgeberkreis des Teubner Verlags Prof Dr Appelrath Prof Dr Waldschmidt und Prof Dr Richter Mein besonderer Dank gilt auch Frau Christiane Hamel Siebdrat f r die Eingabe des Manuskripts in das Textsystem Herrn Friedhelm Mei f r die An fertigung der Bilder meinem Kollegen Dr Ulrich Frank der bei Problemen mit dem Textsystem jederzeit mit Rat und Tat behilflich war sowie den zahlreichen Korrekturlesern aus dem Kollegen und Bekanntenkreis Das Buch stellt den Versuch einer Zwischenbilanz der Forschung dar die sich in den letzten Jahren mit den Problemen der Datenhaltung in CAD Systemen f r den Entwurf hochintegrierter Schaltungen auseinandergesetzt hat Da diese Forschungsarbeiten andauern kann es sich nur um eine Zwischenbilanz handeln die vorzunehmen aber meiner Ansicht nach sinnvoll ist da inzwischen eine gro e Vielfalt von L sungsans tzen existiert ohne da schon erkennbar ist welche sich in der Praxis letztlich als tragf hig erweisen werden Das Buch stellt weiterhin den Versuch dar eine Grundlage f r das gegenseitige Verst ndnis der beiden Entwicklergruppen zu legen die zur L sung der Probleme beitragen m ssen n mlich die Entwickler von Entwurfswerkzeugen einerseits und die Entwickler vonDatenbanksystemen andererseits

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