

Experiment 1. Digital circuit fault diagnosis: Pseudo-exhaustive test

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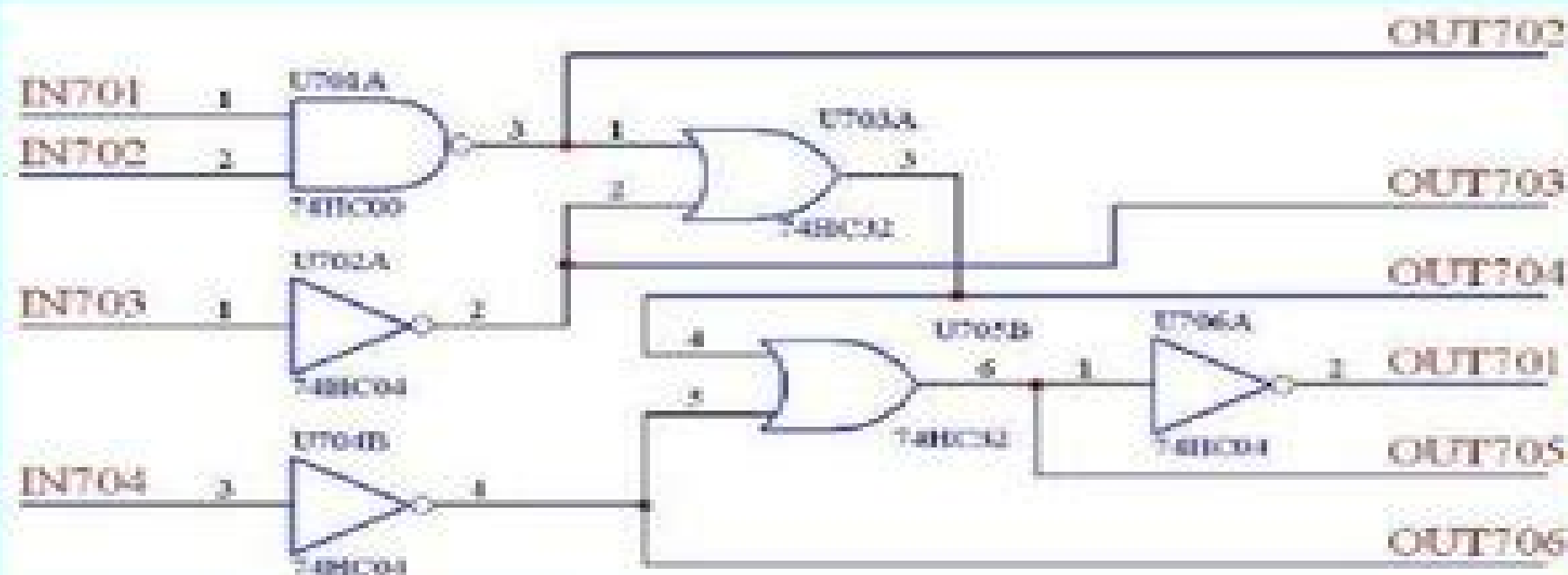


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Fault Diagnosis Of Digital Circuits

Benjamin Rogel Favila



Fault Diagnosis Of Digital Circuits:

Fault Diagnosis of Digital Circuits V. N. Yarmolik, 1990 The continual explosion of computer development has led to inadequate coverage of proper useful on line testing techniques This text fills the gap in the literature by presenting the latest techniques available for digital devices used in the most popular computers Initial chapters explore the classic problems of on line testing pointing out the limited applications of conventional approaches to the problem of diagnosing digital devices using LSI VLSI chips Chapters 4 7 cover compact testing methods used to diagnose complex digital circuits Chapters 8 9 analyze the techniques of compressing output responses of a digital circuit while chapter 10 surveys promising recent signature generation techniques for binary sequences The final chapter covers multi output digital circuits Fault Diagnosis in Digital Circuits Mohamed Saled Soliman Mahmoud, 2017 The goals of fault diagnosis are to ascertain whether faults are present in fault detection and to identify them fault location Fault location is commonly performed with the aid of a fault dictionary Fault dictionaries are constructed via fault simulation under the single fault assumption The single fault model often assumes a circuit is tested often enough such that no more than one physical defect is likely to occur between two consecutive test applications This strategy is not valid when one physical defect manifests itself as multiple faults It is observed that the presence of redundant faults also invalidates the frequent testing strategy since a redundant fault may mask the existence of a detectable fault In all these situations a multiple fault model is required However in almost all practical cases a fault dictionary for multiple faults is infeasible to generate due to an exponential number of equivalence classes In this dissertation we first present a VHDL based CAD tool that integrates design error injection simulation and diagnosis for digital circuits The tool uses an FPGA based board to inject error models in the design and compute the error free and erroneous signatures of internal lines The signatures are later used for detection and diagnosis of errors for the circuit under test CUT Several experiments were conducted to demonstrate the capabilities of the tool The obtained results demonstrate that the tool could detect and locate the source faulty node s within the CUT Then a new approach for a developed fault diagnosis method Our approach is based on an enhanced deduction algorithm which processes the actual response effect of CUT to determine fault situations causes The main tool of our approach processes the response to deduce the internal signal values A multiple stuck at fault model is implicitly employed and no fault enumeration is required The enhanced deduction algorithm is applicable to complicated combinational circuits The internal values obtained are used to determine fault situations in CUT compatible with the applied test T and the response Our analysis can identify fault locations and values s a 0 or s a 1 Our main result is that any stuck fault can be diagnosed Preliminary results demonstrate that our technique always achieves great accuracy for detecting and locating the faults saving a large amount of time especially for more complicated combinational circuits The problems solved by our procedure are using deterministic test vectors We next present a new approach for a developed fault diagnosis method Our approach is based on an enhanced

deduction algorithm and a backtracking strategy which can be regarded as a recursive process of value justification in which we first justify explain the values obtained at the primary outputs POs To justify a 0 value on the output of a NAND gate assuming it is normal we need all the gate inputs to be 1 To justify a 1 value we need at least one input to have value 0 All the known values of internal normal lines must be justified by values of their predecessors When both 0 and 1 values have been deduced for a gate output and it is critical it is identified as normal and all its currently known values are analyzed In some cases we need to decide to select one of the possible ways to justify a 1 value on the output of a NAND gate If a decision leads to an inconsistency self contradictory state with the forward propagated value the algorithm will backtrack to the last decision point and try an alternative decision After a decision is made all the implications resulting from that decision are performed If no inconsistency is detected a new decision point is necessary Otherwise a solution has been obtained A solution is a set of values which could have occurred in the CUT that is a possible set of actual values The main tool of our approach processes the response to deduce the internal signal values in all possible solutions

Digital Circuit Testing and Testability Parag K. Lala,1997 An easy to use introduction to the practices and techniques in the field of digital circuit testing Lala writes in a user friendly and tutorial style making the book easy to read even for the newcomer to fault tolerant system design Each informative chapter is self contained with little or no previous knowledge of a topic assumed Extensive references follow each chapter

Fault Diagnosis of Digital Circuits Mary Alice King,1976 **Fault Diagnosis in Digital Circuits Based on Effect Cause Analysis** Miron Abramovici,1980 **Fault Detection in Digital Circuits** Arthur D. Friedman,Premachandran R. Menon,1971 Model-based Fault Diagnosis of Digital Circuits Benjamin Rogel Favila,1991

A Diagnostic Computer System for Fault Diagnosis of Digital Circuits Fredric Rowland Boswell,1972 *Using logic programming for fault diagnosis in digital circuits* Helmut Simonis,Mehmet Dincbas,1986 Fault Diagnosis of Digital Systems Herbert Y. Chang,Eric Manning,Gernot Metze,1974 Fault Diagnosis in Digital Circuits by Compression Techniques Saeed M. Chaudhry,1994 **Fault Detection and Diagnosis in Digital Circuits and Systems** ,1970*

Fault Diagnosis in Combinational Digital Circuits Suman Jolly,1971 **Fault Diagnosis of Analog Integrated Circuits** Prithviraj Kabisatpathy,Alok Barua,Satyabroto Sinha,2006-01-13 System on Chip SOC having both digital and analog circuits has become increasingly prevalent in integrated circuit manufacturing industry Electronic tests are classified as digital analog and mixed signal Current methodologies for the testing of digital circuits are well developed In contrast methodologies for the testing of analog circuits remain relatively underdeveloped due to the complex nature of analog signals Compared to digital testing analog testing lags far behind in methodologies and tools and therefore demands substantial research and development effort Fault Diagnosis of Analog Integrated Circuits is a textbook for advanced undergraduate and graduate level students as well as practicing engineers The objective of this book is to study the testing and fault diagnosis of analog and analog part of mixed signal circuits A background in analog integrated circuit artificial neural network is

desirable but not essential The text covers the testing and fault diagnosis of both bipolar and Metal Oxide Semiconductor MOS circuits Fault model of the devices in analog domain has been introduced in the text The test stimulus generations are also discussed in details Experimental verification of some state of the art techniques has also been presented in the book It also contains problems that can be used as quiz or homework This book enables the reader to test an analog circuit that is implemented either in bipolar or MOS technology

A Neural Network Model for Fault-diagnosis of Digital Circuits Sridhar S. Ramanujam,1990

Testing and Diagnosis of Analog Circuits and Systems Ruey-wen Liu,2012-12-06

IS THE TOPIC ANALOG TESTING AND DIAGNOSIS TIMELY Yes indeed it is Testing and Diagnosis is an important topic and fulfills a vital need for the electronic industry The testing and diagnosis of digital electronic circuits has been successfully developed to the point that it can be automated Unfortunately its development for analog electronic circuits is still in its Stone Age The engineer's intuition is still the most powerful tool used in the industry There are two reasons for this One is that there has been no pressing need from the industry Analog circuits are usually small in size Sometimes the engineer's experience and intuition are sufficient to fulfill the need The other reason is that there are no breakthrough results from academic research to provide the industry with critical ideas to develop tools This is not because of a lack of effort Both academic and industrial research groups have made major efforts to look into this problem Unfortunately the problem for analog circuits is fundamentally different from and much more difficult than its counterpart for digital circuits These efforts have led to some important findings but are still not at the point of being practically useful However these situations are now changing The current trend for the design of VLSI chips is to use analog digital hybrid circuits instead of digital circuits from the past Therefore even Ixx Preface though the analog circuit may be small the total circuit under testing is large

Testing of Digital Systems N. K. Jha,S. Gupta,2003-05-08

Device testing represents the single largest manufacturing expense in the semiconductor industry costing over 40 billion a year The most comprehensive and wide ranging book of its kind Testing of Digital Systems covers everything you need to know about this vitally important subject Starting right from the basics the authors take the reader through automatic test pattern generation design for testability and built in self test of digital circuits before moving on to more advanced topics such as IDDQ testing functional testing delay fault testing memory testing and fault diagnosis The book includes detailed treatment of the latest techniques including test generation for various fault models discussion of testing techniques at different levels of integrated circuit hierarchy and a chapter on system on a chip test synthesis Written for students and engineers it is both an excellent senior graduate level textbook and a valuable reference

Rational Fault Analysis Richard Saeks,Stanley R. Liberty,1977

Information on the development of rational procedures for detection location prediction of faults in a variety of systems Includes a chapter on computer aided fault analysis

Random Testing of Digital Circuits Rene David,2020-11-26

Introduces a theory of random testing in digital circuits for the first time and offers practical guidance for the implementation of random pattern generators signature

analyzers design for random testability and testing results Contains several new and unpublished results Digital Circuit Testing Francis C. Wong, 2012-12-02 Recent technological advances have created a testing crisis in the electronics industry smaller more highly integrated electronic circuits and new packaging techniques make it increasingly difficult to physically access test nodes New testing methods are needed for the next generation of electronic equipment and a great deal of emphasis is being placed on the development of these methods Some of the techniques now becoming popular include design for testability DFT built in self test BIST and automatic test vector generation ATVG This book will provide a practical introduction to these and other testing techniques For each technique introduced the author provides real world examples so the reader can achieve a working knowledge of how to choose and apply these increasingly important testing methods

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Table of Contents Fault Diagnosis Of Digital Circuits

1. Understanding the eBook Fault Diagnosis Of Digital Circuits
 - The Rise of Digital Reading Fault Diagnosis Of Digital Circuits
 - Advantages of eBooks Over Traditional Books
2. Identifying Fault Diagnosis Of Digital Circuits
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Fault Diagnosis Of Digital Circuits
 - User-Friendly Interface
4. Exploring eBook Recommendations from Fault Diagnosis Of Digital Circuits
 - Personalized Recommendations
 - Fault Diagnosis Of Digital Circuits User Reviews and Ratings
 - Fault Diagnosis Of Digital Circuits and Bestseller Lists
5. Accessing Fault Diagnosis Of Digital Circuits Free and Paid eBooks
 - Fault Diagnosis Of Digital Circuits Public Domain eBooks
 - Fault Diagnosis Of Digital Circuits eBook Subscription Services
 - Fault Diagnosis Of Digital Circuits Budget-Friendly Options

6. Navigating Fault Diagnosis Of Digital Circuits eBook Formats
 - ePub, PDF, MOBI, and More
 - Fault Diagnosis Of Digital Circuits Compatibility with Devices
 - Fault Diagnosis Of Digital Circuits Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Fault Diagnosis Of Digital Circuits
 - Highlighting and Note-Taking Fault Diagnosis Of Digital Circuits
 - Interactive Elements Fault Diagnosis Of Digital Circuits
8. Staying Engaged with Fault Diagnosis Of Digital Circuits
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Fault Diagnosis Of Digital Circuits
9. Balancing eBooks and Physical Books Fault Diagnosis Of Digital Circuits
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Fault Diagnosis Of Digital Circuits
10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
11. Cultivating a Reading Routine Fault Diagnosis Of Digital Circuits
 - Setting Reading Goals Fault Diagnosis Of Digital Circuits
 - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Fault Diagnosis Of Digital Circuits
 - Fact-Checking eBook Content of Fault Diagnosis Of Digital Circuits
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
 - Integration of Multimedia Elements

- Interactive and Gamified eBooks

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