



Fault Detection in Digital Circuits (Computer Applications in Electrical Engineering)

Friedman, Arthur D.

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Fault Detection In Digital Circuits

Nicola DiToro

A decorative red circular graphic with a gradient, appearing as a partial circle or a thick arc, located to the right of the author's name.

Fault Detection In Digital Circuits:

Fault Detection in Digital Circuits Arthur D. Friedman, Premachandran R. Menon, 1971 **Digital Circuit Testing and Testability** Parag K. Lala, 1997 An easy to use introduction to the practices and techniques in the field of digital circuit testing Lala writes in a user friendly and tutorial style making the book easy to read even for the newcomer to fault tolerant system design Each informative chapter is self contained with little or no previous knowledge of a topic assumed Extensive references follow each chapter Fault Diagnosis in Digital Circuits Mohamed Saled Soliman Mahmoud, 2017 The goals of fault diagnosis are to ascertain whether faults are present in fault detection and to identify them fault location Fault location is commonly performed with the aid of a fault dictionary Fault dictionaries are constructed via fault simulation under the single fault assumption The single fault model often assumes a circuit is tested often enough such that no more than one physical defect is likely to occur between two consecutive test applications This strategy is not valid when one physical defect manifests itself as multiple faults It is observed that the presence of redundant faults also invalidates the frequent testing strategy since a redundant fault may mask the existence of a detectable fault In all these situations a multiple fault model is required However in almost all practical cases a fault dictionary for multiple faults is infeasible to generate due to an exponential number of equivalence classes In this dissertation we first present a VHDL based CAD tool that integrates design error injection simulation and diagnosis for digital circuits The tool uses an FPGA based board to inject error models in the design and compute the error free and erroneous signatures of internal lines The signatures are later used for detection and diagnosis of errors for the circuit under test CUT Several experiments were conducted to demonstrate the capabilities of the tool The obtained results demonstrate that the tool could detect and locate the source faulty node s within the CUT Then a new approach for a developed fault diagnosis method Our approach is based on an enhanced deduction algorithm which processes the actual response effect of CUT to determine fault situations causes The main tool of our approach processes the response to deduce the internal signal values A multiple stuck at fault model is implicitly employed and no fault enumeration is required The enhanced deduction algorithm is applicable to complicated combinational circuits The internal values obtained are used to determine fault situations in CUT compatible with the applied test T and the response Our analysis can identify fault locations and values s a 0 or s a 1 Our main result is that any stuck fault can be diagnosed Preliminary results demonstrate that our technique always achieves great accuracy for detecting and locating the faults saving a large amount of time especially for more complicated combinational circuits The problems solved by our procedure are using deterministic test vectors We next present a new approach for a developed fault diagnosis method Our approach is based on an enhanced deduction algorithm and a backtracking strategy which can be regarded as a recursive process of value justification in which we first justify explain the values obtained at the primary outputs POs To justify a 0 value on the output of a NAND gate assuming it is normal we need all the gate inputs to be 1 To justify a 1 value we need at least one input to have value 0 All the

known values of internal normal lines must be justified by values of their predecessors When both 0 and 1 values have been deduced for a gate output and it is critical it is identified as normal and all its currently known values are analyzed In some cases we need to decide to select one of the possible ways to justify a 1 value on the output of a NAND gate If a decision leads to an inconsistency self contradictory state with the forward propagated value the algorithm will backtrack to the last decision point and try an alternative decision After a decision is made all the implications resulting from that decision are performed If no inconsistency is detected a new decision point is necessary Otherwise a solution has been obtained A solution is a set of values which could have occurred in the CUT that is a possible set of actual values The main tool of our approach processes the response to deduce the internal signal values in all possible solutions *Fault Detection and Diagnosis in Digital Circuits and Systems*, 1970* *FAULT DETECTION IN DIGITAL CIRCUITS* Franklin F. Kuo, 1971

Fault Detection in Multi-valued Digital Circuits Huizhu Lu, 1983 Fault Detection In Digital Circuits Friedman A.D.,

Rational Fault Analysis Richard Saeks, Stanley R. Liberty, 1977 Information on the development of rational procedures for detection location prediction of faults in a variety of systems Includes a chapter on computer aided fault analysis

Multiple Fault Detection in Digital Circuits Anastasios S. Vergis, 1984 **DIGITAL ELECTRONICS AND LOGIC**

DESIGN B. SOMANATHAN NAIR, 2002-01-01 Designed as a textbook for undergraduate students in Electrical Engineering Electronics Computer Science and Information Technology this up to date well organized study gives an exhaustive treatment of the basic principles of Digital Electronics and Logic Design It aims at bridging the gap between these two subjects The many years of teaching undergraduate and postgraduate students of engineering that Professor Somanathan Nair has done is reflected in the in depth analysis and student friendly approach of this book Concepts are illustrated with the help of a large number of diagrams so that students can comprehend the subject with ease Worked out examples within the text illustrate the concepts discussed and questions at the end of each chapter drill the students in self study

Detection of Intermittent Faults in Sequential Circuits Stanford University Stanford Electronics Laboratories. Digital Systems Laboratory, J. Savir, 1978 Testing for intermittent faults in digital circuits has been given significant attention in the past few years However very little theoretical work was done regarding their detection in sequential circuits Fault Diagnosis of Digital Circuits V. N. Yarmolik, 1990 The continual explosion of computer development has led to inadequate coverage of proper useful on line testing techniques This text fills the gap in the literature by presenting the latest techniques available for digital devices used in the most popular computers Initial chapters explore the classic problems of on line testing pointing out the limited applications of conventional approaches to the problem of diagnosing digital devices using LSI VLSI chips Chapters 4 7 cover compact testing methods used to diagnose complex digital circuits Chapters 8 9 analyze the techniques of compressing output responses of a digital circuit while chapter 10 surveys promising recent signature generation techniques for binary sequences The final chapter covers multi output digital circuits **Fault**

Diagnosis of Analog Integrated Circuits Prithviraj Kabisatpathy, Alok Barua, Satyabroto Sinha, 2006-01-13 System on Chip SOC having both digital and analog circuits has become increasingly prevalent in integrated circuit manufacturing industry. Electronic tests are classified as digital, analog, and mixed signal. Current methodologies for the testing of digital circuits are well developed. In contrast, methodologies for the testing of analog circuits remain relatively underdeveloped due to the complex nature of analog signals. Compared to digital testing, analog testing lags far behind in methodologies and tools and therefore demands substantial research and development effort. *Fault Diagnosis of Analog Integrated Circuits* is a textbook for advanced undergraduate and graduate level students as well as practicing engineers. The objective of this book is to study the testing and fault diagnosis of analog and analog part of mixed signal circuits. A background in analog integrated circuit, artificial neural network is desirable but not essential. The text covers the testing and fault diagnosis of both bipolar and Metal Oxide Semiconductor MOS circuits. Fault model of the devices in analog domain has been introduced in the text. The test stimulus generations are also discussed in details. Experimental verification of some state of the art techniques has also been presented in the book. It also contains problems that can be used as quiz or homework. This book enables the reader to test an analog circuit that is implemented either in bipolar or MOS technology. *The Sign Transform's Application of Fault Detection in Digital Circuits and Its Efficient Implementation* Nicola DiToro, 1991

Digital Circuit Testing Francis C. Wong, 2012-12-02 Recent technological advances have created a testing crisis in the electronics industry. Smaller, more highly integrated electronic circuits and new packaging techniques make it increasingly difficult to physically access test nodes. New testing methods are needed for the next generation of electronic equipment and a great deal of emphasis is being placed on the development of these methods. Some of the techniques now becoming popular include design for testability, DFT, built-in self test, BIST, and automatic test vector generation, ATVG. This book will provide a practical introduction to these and other testing techniques. For each technique introduced, the author provides real world examples so the reader can achieve a working knowledge of how to choose and apply these increasingly important testing methods.

Random Testing of Digital Circuits Rene David, 2020-11-26 Introduces a theory of random testing in digital circuits for the first time and offers practical guidance for the implementation of random pattern generators, signature analyzers, design for random testability, and testing results. Contains several new and unpublished results.

Workshop on Fault Detection & Diagnosis in Digital Circuits & Systems Lehigh University. Department of Electrical Engineering, Institute of Electrical and Electronics Engineers. Lehigh Valley Section, 1971*

Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits M. Bushnell, Vishwani Agrawal, 2006-04-11 The modern electronic testing has a forty year history. Test professionals hold some fairly large conferences and numerous workshops have a journal and there are over one hundred books on testing. Still a full course on testing is offered only at a few universities, mostly by professors who have a research interest in this area. Apparently most professors would not have taken a course on electronic testing when they were

students Other than the computer engineering curriculum being too crowded the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook For VLSI the foundation was provided by semiconductor device technology circuit design and electronic testing In a computer engineering curriculum therefore it is necessary that foundations should be taught before applications The field of VLSI has expanded to systems on a chip which include digital memory and mixed signalsubsystems To our knowledge this is the first textbook to cover all three types of electronic circuits We have written this textbook for an undergraduate foundations course on electronic testing Obviously it is too voluminous for a one semester course and a teacher will have to select from the topics We did not restrict such freedom because the selection may depend upon the individual expertise and interests Besides there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course With equal tenacity we address the needs of three other groups of readers

Spectral Techniques and Fault Detection Marg Karpovsky, 2012-12-02 Spectral Techniques and Fault Detection focuses on the spectral techniques for the analysis testing and design of digital devices This book discusses the error detection and correction in digital devices Organized into 10 chapters this book starts with an overview of the concepts and tools to evaluate the applicability of various spectral approaches and fault detection techniques to the design This text then describes the class of generalized Programmable Logic Array configurations called Encoded PLAs Other chapters consider the two sided Chrestenson Transform to the analysis of some pattern properties This book describes as well a certain type of cellular arrays for highly parallel processing namely three dimensional arrays The final chapter deals with the system design methods that allow and encourage designers to incorporate the necessary distributed error correction throughout any digital system This book is a valuable resource for graduate students and engineers working in the fields of logic design spectral techniques testing and self testing of digital devices

Fault Diagnosis of Digital Systems Herbert Y. Chang, Eric Manning, Gernot Metze, 1974

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