Fault Tolerance Through Reconfiguration in VLSI and WSI Arrays (Computer Systems Series)

Negrini

Fault Tolerance Through Reconfiguration In Vlsi And Wsi Arrays

Marco Cascella

Fault Tolerance Through Reconfiguration In Vlsi And Wsi Arrays:

Fault-tolerance Through Reconfiguration of VLSI and WSI Arrays R. Negrini,Mariagiovanna Sami,Renato Stefanelli,1989 This book brings together and discusses the most significant results scattered across the vast field of research in fault tolerance   **Defect and Fault Tolerance in VLSI Systems** Israel Koren,2012-12-06 This book contains an edited selection of papers presented at the International Workshop on Defect and Fault Tolerance in VLSI Systems held October 6 7 1988 in Springfield Massachusetts Our thanks go to all the contributors and especially the members of the program committee for the difficult and time consuming work involved in selecting the papers that were presented in the workshop and reviewing the papers included in this book Thanks are also due to the IEEE Computer Society in particular the Technical Committee on Fault Tolerant Computing and the Technical Committee on VLSI and the University of Massachusetts at Amherst for sponsoring the workshop and to the National Science Foundation for supporting under grant number MIP 8803418 the keynote address and the distribution of this book to all workshop attendees The objective of the workshop was to bring t ogether researchers and practition ers from both industry and academia in the field of defect tolerance and yield en ha ncement in VLSI to discuss their mutual interests in defect tolerant architectures and models for integrated circuit defects faults and yield Progress in this area was slowed down by the proprietary nature of yield related data and by the lack of appropriate forums for disseminating such information The goal of this workshop was therefore to provide a forum for a dialogue and exchange of views A follow up workshop in October 1989 with C H Stapper from IBM and V K Jain from the University of South Florida as general co chairmen is being organized   **Self-restructuring in Fault Tolerant Architecture** Itsuo Takanami,2025-04-16 Recently high speed and high quality technologies for processing many kinds of information have become essential and will become more and more necessary in the future For such needs parallel computer systems composed of many processing elements PEs are used and it is important to make high reliable systems which is called fault tolerant computer systems As VLSI technology has developed the realization of parallel computer systems using multi chip module MCM or wafer scale integration WSI has been considered so as to enhance the speed of the computers decrease energy consumption and sizes and so on In such a realization entire or significant parts of PEs and connections among them are connected or implemented on a board or wafer Therefore the reliability and or yield of the system may become drastically low if there is no strategy for coping with faults or defects In realizing such systems as well as parallel computer systems in order to restore the correct computation capabilities of the systems with faults it must be reconfigured appropriately using spare PEs so that the faulty PEs are eliminated from the computation paths by replacing faulty PEs with healthy spare PEs and the remaining healthy PEs maintain correct logical connectivity among them Various strategies to reconfigure a faulty physical system into a fault free target logical system are described in the literature Some of these techniques employ very powerful reconfiguring systems that can repair a faulty processor array with almost

certainty even in the presence of clusters of multiple faults However the key limitation of these techniques is that they are executed in software programs to run on an external host computer and they cannot be designed and implemented efficiently within a system If a faulty system can be self reconfigured by a built in circuit or network the system down time is significantly reduced Furthermore the system will become more reliable when it is used in such environments that the fault information cannot be monitored externally and manual maintenance operations are difficult This book concerns fault tolerant systems consisting of many PEs mainly mesh connected processor arrays A mesh connected processor array is a kind of form of massively parallel computing systems which consist of hundreds of PEs and have regular and modular structures small wiring length between PEs and high scalabilities Here self reconfiguration of processor systems with spares using built in digital circuits are focused on and spare arrangements together with networks connecting among PEs and reconfiguration algorithms with digital circuits are described considering the number of spares reconfiguration algorithms and their hardware realizations built in circuits etc where spares are arranged on the sides or diagonal of arrays The effectiveness of the systems is evaluated in terms of the survival rates successfully reconfigured rates for the number of faults and the array reliabilities successfully reconfigured probabilities under the condition that each PE is equally reliable   *Defect and Fault Tolerance in VLSI Systems* C.H. Stapper,V.K. Jain,Gabriele Saucier,2013-06-29 Higher circuit densities increasingly more complex application ohjectives and advanced packaging technologies have suhstantially increased the need to incorporate defect tolerance and fault tolerance in the design of VLSI and WSI systems The goals of defect tolerance and fault tolerance are yield enhancement and improved reliahility The emphasis on this area has resulted in a new field of interdisciplinary scientific research I n fact advanced methods of defect fault control and tolerance are resulting in enhanced manufacturahility and productivity of integrated circuit chips VI SI systems and wafer scale integrated circuits In 1987 Dr W Moore organized an International Workshop on Designing for Yield at Oxford University Edited papers of that workshop were published in reference II The participants in that workshop agreed that meetings of this type should he con tinued preferahly on a yearly hasis It was Dr I Koren who organized the IEEE Inter national Workshop on Defect and Fault Tolerance in VLSI Systems in Springfield Massachusetts the next year Selected papers from that workshop were puhlished as the first volume of this series 21   **Computational Science - ICCS 2003. Part 3.** Peter Sloot,2003-05-22 The four volume set LNCS 2657 LNCS 2658 LNCS 2659 and LNCS 2660 constitutes the refereed proceedings of the Third International Conference on Computational Science ICCS 2003 held concurrently in Melbourne Australia and in St Petersburg Russia in June 2003 The four volumes present more than 460 reviewed contributed and invited papers and span the whole range of computational science from foundational issues in computer science and algorithmic mathematics to advanced applications in virtually all application fields making use of computational techniques These proceedings give a unique account of recent results in the field   <u>Transactions on Computational Science XXXIV</u> Marina L. Gavrilova,C.J. Kenneth Tan,2019-08-28 The LNCS journal

Transactions on Computational Science reflects recent developments in the field of Computational Science conceiving the field not as a mere ancillary science but rather as an innovative approach supporting many other scientific disciplines The journal focuses on original high quality research in the realm of computational science in parallel and distributed environments encompassing the facilitating theoretical foundations and the applications of large scale computations and massive data processing It addresses researchers and practitioners in areas ranging from aerospace to biochemistry from electronics to geosciences from mathematics to software architecture presenting verifiable computational methods findings and solutions and enabling industrial users to apply techniques of leading edge large scale high performance computational methods This the 34th issue of the Transactions on Computational Science contains seven in depth papers focusing on research on data analytics using machine learning and pattern recognition with applications in wireless networks databases and remotely sensed data   Transactions on Computational Science XXXIX Marina L. Gavrilova,C. J. Kenneth Tan,2023-01-01 The LNCS journal Transactions on Computational Science reflects recent developments in the field of Computational Science conceiving the field not as a mere ancillary science but rather as an innovative approach supporting many other scientific disciplines The journal focuses on original high quality research in the realm of computational science in parallel and distributed environments encompassing the facilitating theoretical foundations and the applications of large scale computations and massive data processing It addresses researchers and practitioners in areas ranging from aerospace to biochemistry from electronics to geosciences from mathematics to software architecture presenting verifiable computational methods findings and solutions and enabling industrial users to apply techniques of leading edge large scale high performance computational methods This the 39th issue of the Transactions on Computational Science is devoted to research on geometric modeling visual object detection cloud service utilization pattern recognition processing arrays and classification using bio heuristic optimization   Transactions on Computational Science XXXVIII Marina L. Gavrilova,C.J. Kenneth Tan,2021-03-24 The LNCS journal Transactions on Computational Science reflects recent developments in the field of Computational Science conceiving the field not as a mere ancillary science but rather as an innovative approach supporting many other scientific disciplines The journal focuses on original high quality research in the realm of computational science in parallel and distributed environments encompassing the facilitating theoretical foundations and the applications of large scale computations and massive data processing It addresses researchers and practitioners in areas ranging from aerospace to biochemistry from electronics to geosciences from mathematics to software architecture presenting verifiable computational methods findings and solutions and enabling industrial users to apply techniques of leading edge large scale high performance computational methods This the 38th issue of the Transactions on Computational Science is devoted to research on modelling optimization and graphs with applications in 3D and sketch modelling engineering design evolutionary computing and networks   **Design And Analysis Of Reliable And Fault-tolerant**

Computer Systems Mostafa I Abd-el-barr,2006-12-15 Covering both the theoretical and practical aspects of fault tolerant mobile systems and fault tolerance and analysis this book tackles the current issues of reliability based optimization of computer networks fault tolerant mobile systems and fault tolerance and reliability of high speed and hierarchical networks The book is divided into six parts to facilitate coverage of the material by course instructors and computer systems professionals The sequence of chapters in each part ensures the gradual coverage of issues from the basics to the most recent developments A useful set of references including electronic sources is listed at the end of each chapter a

Transactions on Computational Science XXVII Marina L. Gavrilova,C.J. Kenneth Tan,2016-04-07 The LNCS journal Transactions on Computational Science reflects recent developments in the field of Computational Science conceiving the field not as a mere ancillary science but rather as an innovative approach supporting many other scientific disciplines The journal focuses on original high quality research in the realm of computational science in parallel and distributed environments encompassing the facilitating theoretical foundations and the applications of large scale computations and massive data processing It addresses researchers and practitioners in areas ranging from aerospace to biochemistry from electronics to geosciences from mathematics to software architecture presenting verifiable computational methods findings and solutions and enabling industrial users to apply techniques of leading edge large scale high performance computational methods This the 27th issue of the Transactions on Computational Science journal is devoted to the topic of high performance computing It contains eight full papers covering the areas of cloud middleware multi processor systems quantum computing optimization and secure biometric based encryption methods   Computer Arithmetics for Nanoelectronics Vlad P. Shmerko,Svetlana N. Yanushkevich,Sergey Edward Lyshevski,2018-10-03 Emphasizes the Basic Principles of Computational Arithmetic and Computational Structure Design Taking an interdisciplinary approach to the nanoscale generation of computer devices and systems Computer Arithmetics for Nanoelectronics develops a consensus between computational properties provided by data structures and phenomenological properties of nano and molecular technology Covers All Stages of the Design Cycle from Task Formulation to Molecular Based Implementation The book introduces the theoretical base and properties of various data structures along with techniques for their manipulation optimization and implementation It also assigns the computational properties of logic design data structures to 3D structures furnishes information theoretical measures and design aspects and discusses the testability problem The last chapter presents a nanoscale prospect for natural computing based on assorted computing paradigms from nature Balanced Coverage of State of the Art Concepts Techniques and Practices Up to date comprehensive and pragmatic in its approach this text provides a unified overview of the relationship between the fundamentals of digital system design computer architectures and micro and nanoelectronics   On-Line Testing for VLSI Michael Nicolaidis,Yervant Zorian,Dhiraj Pradhan,2013-03-09 Test functions fault detection diagnosis error correction repair etc that are applied concurrently while

the system continues its intended function are defined as on line testing In its expanded scope on line testing includes the design of concurrent error checking subsystems that can be themselves self checking fail safe systems that continue to function correctly even after an error occurs reliability monitoring and self test and fault tolerant designs On Line Testing for VLSI contains a selected set of articles that discuss many of the modern aspects of on line testing as faced today The contributions are largely derived from recent IEEE International On Line Testing Workshops Guest editors Michael Nicolaidis Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties On Line Testing for VLSI is an edited volume of original research comprising invited contributions by leading researchers **Fault-Tolerant Computing Systems** Mario Dal Cin,Wolfgang Hohl,2012-12-06 5th International GI ITG GMA Conference N rnberg September 25 27 1991 Proceedings **Pyramidal Systems for Computer Vision** Virginio Cantoni,Stefano Levialdi,2012-12-06 This book contains the proceedings of the NATO Advanced Research Workshop held in Maratea Italy May 5 9 1986 on Pyramidal Systems for Image Processing and Computer Vision We had 40 participants from 11 countries playing an active part in the workshop and all the leaders of groups that have produced a prototype pyramid machine or a design for such a machine were present Within the wide field of parallel architectures for image processing a new area was recently born and is growing healthily the area of pyramidally structured multiprocessing systems Essentially the processors are arranged in planes from a base to an apex each one of which is generally a reduced usually by a power of two version of the plane underneath these processors are horizontally interconnected within a plane and vertically connected with fathers on top planes and children on the plane below This arrangement has a number of interesting features all of which were amply discussed in our Workshop including the cellular array and hypercube versions of pyramids A number of projects in different parts of the world are reported as well as some interesting applications in computer vision tactile systems and numerical calculations *Electronic Systems and Applications* R. P Agarwal,S Sarkar,1994 *Artificial Life 8* Russell K. Standish,Mark Bedau,Hussein A. Abbass,2003 How high level behaviors arise from low level rules and how understanding this relationship can suggest novel solutions to complex real world problems such as disease prevention stock market prediction and data mining on the Internet The term artificial life describes research into synthetic systems that possess some of the essential properties of life This interdisciplinary field includes biologists computer scientists physicists chemists geneticists and others Artificial life may be viewed as an attempt to understand high level behavior from low level rules for example how the simple interactions between ants and their environment lead to complex trail following behavior An understanding of such relationships in particular systems can suggest novel solutions to complex real world problems such as disease prevention stock market prediction and data mining on the Internet Since their inception in 1987 the Artificial Life meetings have grown from small workshops to truly international conferences reflecting the field s increasing appeal to

researchers in all areas of science   <u>Wafer-Level Integrated Systems</u> Stuart K. Tewksbury,2012-12-06 From the perspective of complex systems conventional Ie s can be regarded as discrete devices interconnected according to system design objectives imposed at the circuit board level and higher levels in the system implementation hierarchy However silicon monolithic circuits have progressed to such complex functions that a transition from a philosophy of integrated circuits Ie s to one of integrated sys tems is necessary Wafer scale integration has played an important role over the past few years in highlighting the system level issues which will most significantly impact the implementation of complex monolithic systems and system components Rather than being a revolutionary approach wafer scale integration will evolve naturally from VLSI as defect avoidance fault tolerance and testing are introduced into VLSI circuits Successful introduction of defect avoidance for example relaxes limits imposed by yield and cost on Ie dimensions allowing the monolithic circuit s area to be chosen according to the natural partitioning of a system into individual functions rather than imposing area limits due to defect densities The term wafer level is perhaps more appropriate than wafer scale A wafer level monolithic system component may have dimensions ranging from conventional yield limited Ie dimensions to full wafer dimensions In this sense wafer scale merely represents the obvious upper practical limit imposed by wafer sizes on the area of monolithic circuits The transition to monolithic wafer level integrated systems will require a mapping of the full range of system design issues onto the design of monolithic circuit   **The Evolution of Fault-Tolerant Computing** A. Avizienis,H. Kopetz,J.C. Laprie,2012-12-06 For the editors of this book as well as for many other researchers in the area of fault tolerant computing Dr William Caswell Carter is one of the key figures in the formation and development of this important field We felt that the IFIP Working Group 10 4 at Baden Austria in June 1986 which coincided with an important step in Bill s career was an appropriate occasion to honor Bill s contributions and achievements by organizing a one day Symposium on the Evolution of Fault Tolerant Computing in the honor of William C Carter The Symposium held on June 30 1986 brought together a group of eminent scientists from all over the world to discuss the evolu tion the state of the art and the future perspectives of the field of fault tolerant computing Historic developments in academia and industry were presented by individuals who themselves have actively been involved in bringing them about The Symposium proved to be a unique historic event and these Proceedings which contain the final versions of the papers presented at Baden are an authentic reference document
   Supercomputing in Engineering Analysis Hojjat Adeli,2020-08-13 The first volume in this new series has a companion in volume 2 unseen Parallel processing in computational mechanics The first six contributions present general aspects of supercomputing from both hardware and software engineering points of view Subsequent chapters discuss homotopy algorithms   *Graph Grammars and Their Application to Computer Science* Janice Cuny,1996-05-08 This book describes the functional properties and the structural organization of the members of the thrombospondin gene family These proteins comprise a family of extracellular calcium binding proteins that modulate cellular adhesion migration and proliferation

Thrombospondin 1 has been shown to function during angiogenesis wound healing and tumor cell metastasis

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