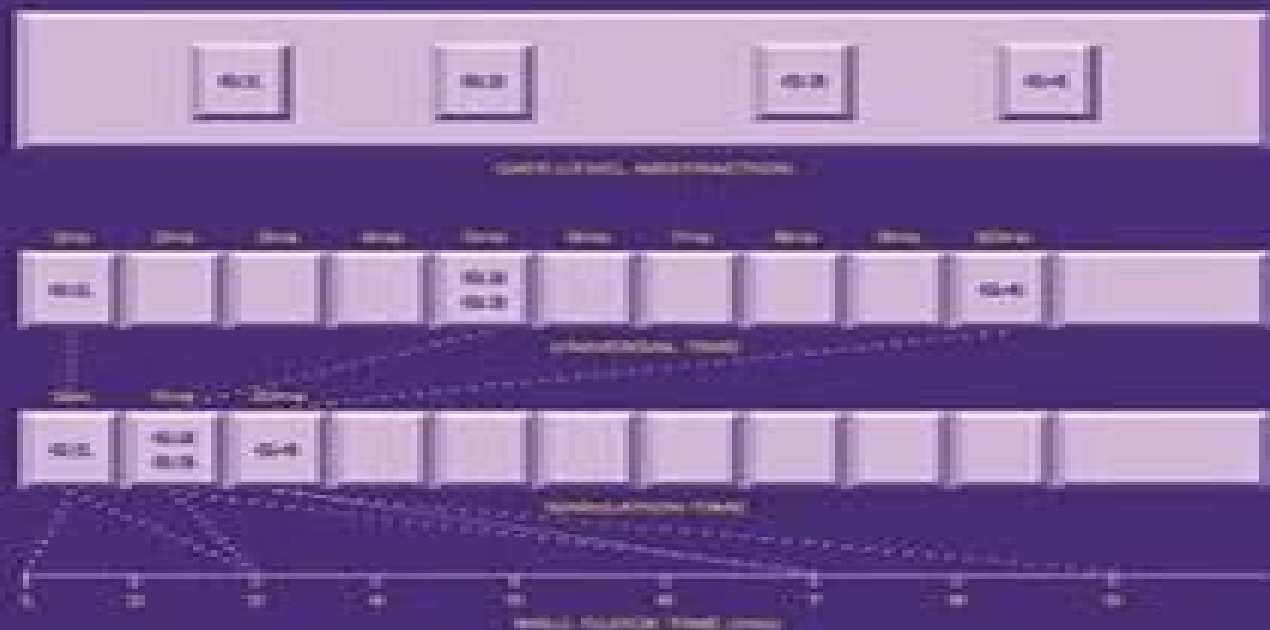


Hardware Description Languages

CONCEPTS AND PRINCIPLES

Sumit Ghosh



IEEE Press Series on
Microelectronic Systems

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Series Editors

Hardware Description Languages Concepts And Principles

Sumit Ghosh, Elliot Turrini



Hardware Description Languages Concepts And Principles:

Hardware Description Languages: Concepts And Principles Ghosh, Hardware Description Languages Sumit Ghosh, 2000 Hardware description languages HDLs hold the key to future processor designs but until now no book has offered a clear analysis of the basic principles underlying HDLs **HARDWARE DESCRIPTION LANGUAGES** is the first book to unlock the often hidden science of HDLs along with their origins and basic concepts This indispensable guide explains HDLs and includes an insightful overview of the foremost HDLs of the past three decades from Computer Design Language CDL to Very High Speed Integrated Circuit VHSIC to VHSIC Hardware Description Language VHDL To improve both your knowledge and digital designs of HDL fundamentals this valuable book features these essential topics A critical review of VHDL and Verilog Accurate modeling of hardware Distributed simulation of behavior models New semantics for transport delay **HARDWARE DESCRIPTION LANGUAGES** is written for practicing electronic CAD engineers researchers in simulation and verification of electronic CAD graduate and doctoral students in computer design and undergraduates specializing in electronic hardware design Professors To request an examination copy simply e mail collegeadoption ieee org Sponsored by IEEE Solid State Circuits Council Society IEEE Circuits and Systems Society *Fundamentals and Standards in Hardware Description Languages* Jean Mermet, 2012-12-06 The second half of this century will remain as the era of proliferation of electronic computers They did exist before but they were mechanical During next century they may perform other mutations to become optical or molecular or even biological Actually all these aspects are only fancy dresses put on mathematical machines This was always recognized to be true in the domain of software where machine or high level languages are more or less rigorous but immaterial variations of the universally accepted mathematical language aimed at specifying elementary operations functions algorithms and processes But even a mathematical machine needs a physical support and this is what hardware is all about The invention of hardware description languages HDL s in the early 60 s was an attempt to stay longer at an abstract level in the design process and to push the stage of physical implementation up to the moment when no more technology independent decisions can be taken It was also an answer to the continuous exponential growth of complexity of systems to be designed This problem is common to hardware and software and may explain why the syntax of hardware description languages has followed with a reasonable delay of ten years the evolution of the programming languages at the end of the 60 s they were Algol like a decade later Pascal like and now they are C or ADA like They have also integrated the new concepts of advanced software specification languages **Advanced VLSI Design and Testability Issues** Suman Lata Tripathi, Sobhit Saxena, Sushanta Kumar Mohapatra, 2020-08-19 This book facilitates the VLSI interested individuals with not only in depth knowledge but also the broad aspects of it by explaining its applications in different fields including image processing and biomedical The deep understanding of basic concepts gives you the power to develop a new application aspect which is very well taken care of in this book by using simple language in explaining the concepts In the VLSI world the

importance of hardware description languages cannot be ignored as the designing of such dense and complex circuits is not possible without them Both Verilog and VHDL languages are used here for designing The current needs of high performance integrated circuits ICs including low power devices and new emerging materials which can play a very important role in achieving new functionalities are the most interesting part of the book The testing of VLSI circuits becomes more crucial than the designing of the circuits in this nanometer technology era The role of fault simulation algorithms is very well explained and its implementation using Verilog is the key aspect of this book This book is well organized into 20 chapters Chapter 1 emphasizes on uses of FPGA on various image processing and biomedical applications Then the descriptions enlighten the basic understanding of digital design from the perspective of HDL in Chapters 2 5 The performance enhancement with alternate material or geometry for silicon based FET designs is focused in Chapters 6 and 7 Chapters 8 and 9 describe the study of bimolecular interactions with biosensing FETs Chapters 10 13 deal with advanced FET structures available in various shapes materials such as nanowire HFET and their comparison in terms of device performance metrics calculation Chapters 14 18 describe different application specific VLSI design techniques and challenges for analog and digital circuit designs Chapter 19 explains the VLSI testability issues with the description of simulation and its categorization into logic and fault simulation for test pattern generation using Verilog HDL Chapter 20 deals with a secured VLSI design with hardware obfuscation by hiding the IC s structure and function which makes it much more difficult to reverse engineer

RTL Hardware Design Using VHDL Pong P. Chu, 2006-04-20 The skills and guidance needed to master RTL hardware design This book teaches readers how to systematically design efficient portable and scalable Register Transfer Level RTL digital circuits using the VHDL hardware description language and synthesis software Focusing on the module level design which is composed of functional units routing circuit and storage the book illustrates the relationship between the VHDL constructs and the underlying hardware components and shows how to develop codes that faithfully reflect the module level design and can be synthesized into efficient gate level implementation Several unique features distinguish the book Coding style that shows a clear relationship between VHDL constructs and hardware components Conceptual diagrams that illustrate the realization of VHDL codes Emphasis on the code reuse Practical examples that demonstrate and reinforce design concepts procedures and techniques Two chapters on realizing sequential algorithms in hardware Two chapters on scalable and parameterized designs and coding One chapter covering the synchronization and interface between multiple clock domains Although the focus of the book is RTL synthesis it also examines the synthesis task from the perspective of the overall development process Readers learn good design practices and guidelines to ensure that an RTL design can accommodate future simulation verification and testing needs and can be easily incorporated into a larger system or reused Discussion is independent of technology and can be applied to both ASIC and FPGA devices With a balanced presentation of fundamentals and practical examples this is an excellent textbook for upper level undergraduate or graduate courses in

advanced digital logic Engineers who need to make effective use of today's synthesis software and FPGA devices should also refer to this book *Computer Hardware Description Languages and their Applications* D. Borriore, R. Waxman, 2014-06-28

The topic areas presented within this volume focus on design environments and the applications of hardware description and modelling including simulation verification by correctness proofs synthesis and test The strong relationship between the topics of CHDL 91 and the work around the use and re standardization of the VHDL language is also explored The quality of this proceedings and its significance to the academic and professional worlds is assured by the excellent technical programme here compiled

Modeling and Simulation in Manufacturing and Defense Acquisition National Research Council, Division on Engineering and Physical Sciences, Board on Manufacturing and Engineering Design, Committee on Modeling and Simulation Enhancements for 21st Century Manufacturing and Acquisition, 2002-08-01

The Committee on Modeling and Simulation Enhancements for 21st Century Manufacturing and Acquisition was formed by the NRC in response to a request from the Defense Modeling and Simulation Office DMSO of DOD The committee was asked to

- 1 investigate next generation evolutionary and revolutionary
- 2 identify specific emerging design testing and manufacturing process technologies that can be enabled by advanced
- 3 relate these emerging technologies to long term DOD requirements
- 4 assess ongoing efforts to develop advanced
- 5 identify lessons learned from industry and
- 6 recommend specific government actions to expedite development and to enable maximum DOD and U S commercial benefit from these capabilities

To complete its task the committee identified relevant trends and their impact on defense acquisition needs current use and support for use of lessons learned from commercial manufacturing three cross cutting and especially challenging uses of M and the areas in which basic research is needed in M S in order to achieve the desired goals for manufacturing and defense acquisition

Artificial Intelligence and Simulation Tag G. Kim, 2005-01-31

This book constitutes the refereed post proceedings of the 13th International Conference on AI Simulation and Planning in High Autonomy Systems AIS 2004 held in Jeju Island Korea in October 2004 The 74 revised full papers presented together with 2 invited keynote papers were carefully reviewed and selected from 170 submissions after the conference the papers went through another round of revision The papers are organized in topical sections on modeling and simulation methodologies intelligent control computer and network security HLA and simulator interoperation manufacturing agent based modeling DEVS modeling and simulation parallel and distributed modeling and simulation mobile computer networks Web based simulation and natural systems modeling and simulation environments AI and simulation component based modeling watermarking and semantics graphics visualization and animation and business modeling

Algorithm Design for Networked Information Technology Systems Sumit Ghosh, 2007-05-08

I felt deeply honored when Professor Sumit Ghosh asked me to write the foreword to his book with an extraordinary perspective I have long admired him first as a student leader at Stanford where he initiated the first IEEE Computer Society's student chapter and later as an esteemed and inspiring friend whose transdisciplinary research

broadened and enhanced the horizons of practitioners of computer science and engineering including my own. His ideas which are derived from his profound vision, deep critical thinking and personal intuition reach from information technology to bioscience as exhibited in this excellent book. To me, an ordinary engineer, it opens up a panoramic view of the Universe of Knowledge that keeps expanding and spiraling like the good Indian proverb which says a good book informs you, an excellent book teaches you, and a great book changes you. I sincerely believe that Professor Ghosh's book will help us change and advance the methods of systems engineering and technology. Vision Inspired vision sees ahead of others what will or may come to be a vivid imagined concept or anticipation. An inspired vision personifies what is good and what like minded individuals hope for. Our vision is one of creating an Internet of minds where minds are Web sites or knowledge centers which create, store and radiate knowledge through interaction with other minds connected by a universal shared network. This vision will not just hasten the death of distance but will also carcerate ignorance.

Cybercrimes: A Multidisciplinary Analysis

Sumit Ghosh, Elliot Turrini, 2010-09-22. Designed to serve as a reference work for practitioners, academics and scholars worldwide, this book is the first of its kind to explain complex cybercrimes from the perspectives of multiple disciplines: computer science, law, economics, psychology, etc. and scientifically analyze their impact on individuals, society and nations holistically and comprehensively. In particular, the book shows how multiple disciplines concurrently bring out the complex, subtle and elusive nature of cybercrimes. How cybercrimes will affect every human endeavor at the level of individuals, societies and nations. How to legislate proactive cyberlaws building on a fundamental grasp of computers and networking and stop reacting to every new cyberattack. How conventional laws and traditional thinking fall short in protecting us from cybercrimes. How we may be able to transform the destructive potential of cybercrimes into amazing innovations in cyberspace that can lead to explosive technological growth and prosperity.

CMOS R. Jacob Baker, 2019-05-16. A revised guide to the theory and implementation of CMOS analog and digital IC design. The fourth edition of CMOS Circuit Design, Layout and Simulation is an updated guide to the practical design of both analog and digital integrated circuits. The author, a noted expert on the topic, offers a contemporary review of a wide range of analog/digital circuit blocks including phase-locked loops, delta-sigma sensing circuits, voltage/current references, op-amps, the design of data converters and switching power supplies. CMOS includes discussions that detail the trade-offs and considerations when designing at the transistor level. The companion website contains numerous examples for many computer-aided design (CAD) tools. Using the website enables readers to recreate, modify or simulate the design examples presented throughout the book. In addition, the author includes hundreds of end-of-chapter problems to enhance understanding of the content presented. This newly revised edition provides in-depth coverage of both analog and digital transistor-level design techniques. Discusses the design of phase and delay-locked loops, mixed-signal circuits, data converters and circuit noise. Explores real-world process parameters, design rules and layout examples. Contains a new chapter on Power Electronics. Written for students in electrical and computer engineering and

professionals in the field the fourth edition of CMOS Circuit Design Layout and Simulation is a practical guide to understanding analog and digital transistor level design theory and techniques *Junctionless Field-Effect Transistors* Shubham Sahay, Mamidala Jagadesh Kumar, 2019-02-27 A comprehensive one volume reference on current JLFET methods techniques and research Advancements in transistor technology have driven the modern smart device revolution many cell phones watches home appliances and numerous other devices of everyday usage now surpass the performance of the room filling supercomputers of the past Electronic devices are continuing to become more mobile powerful and versatile in this era of internet of things IoT due in large part to the scaling of metal oxide semiconductor field effect transistors MOSFETs Incessant scaling of the conventional MOSFETs to cater to consumer needs without incurring performance degradation requires costly and complex fabrication process owing to the presence of metallurgical junctions Unlike conventional MOSFETs junctionless field effect transistors JLFETs contain no metallurgical junctions so they are simpler to process and less costly to manufacture JLFETs utilize a gated semiconductor film to control its resistance and the current flowing through it Junctionless Field Effect Transistors Design Modeling and Simulation is an inclusive one stop reference on the study and research on JLFETs This timely book covers the fundamental physics underlying JLFET operation emerging architectures modeling and simulation methods comparative analyses of JLFET performance metrics and several other interesting facts related to JLFETs A calibrated simulation framework including guidance on Sentaurus TCAD software enables researchers to investigate JLFETs develop new architectures and improve performance This valuable resource Addresses the design and architecture challenges faced by JLFET as a replacement for MOSFET Examines various approaches for analytical and compact modeling of JLFETs in circuit design and simulation Explains how to use Technology Computer Aided Design software TCAD to produce numerical simulations of JLFETs Suggests research directions and potential applications of JLFETs Junctionless Field Effect Transistors Design Modeling and Simulation is an essential resource for CMOS device design researchers and advanced students in the field of physics and semiconductor devices **Embedded**

Processor-Based Self-Test Dimitris Gizopoulos, A. Paschalis, Yervant Zorian, 2013-03-09 Embedded Processor Based Self Test is a guide to self testing strategies for embedded processors Embedded processors are regularly used today in most System on Chips SoCs Testing of microprocessors and embedded processors has always been a challenge because most traditional testing techniques fail when applied to them This is due to the complex sequential structure of processor architectures which consists of high performance datapath units and sophisticated control logic for performance optimization Structured Design for Testability DfT and hardware based self testing techniques which usually have a non trivial impact on a circuit s performance size and power can not be applied without serious consideration and careful incorporation into the processor design Embedded Processor Based Self Test shows how the powerful embedded functionality that processors offer can be utilized as a self testing resource Through a discussion of different strategies the book emphasizes on the emerging

area of Software Based Self Testing SBST SBST is based on the idea of execution of embedded software programs to perform self testing of the processor itself and its surrounding blocks in the SoC SBST is a low cost strategy in terms of overhead area speed power development effort and test application cost as it is applied using low cost low speed test equipment Embedded Processor Based Self Test can be used by designers DfT engineers test practitioners researchers and students working on digital testing and in particular processor and SoC test This book sets the framework for comparisons among different SBST methodologies by discussing key requirements It presents successful applications of SBST to a number of embedded processors of different complexities and instruction set architectures

Hardware Description Languages and their Applications

Carlos Delgado Kloos, Eduard Cerny, 2013-06-05 In the past few decades Computer Hardware Description Languages CHDLs have been a rapidly expanding subject area due to a number of factors including the advancing complexity of digital electronics the increasing prevalence of generic and programmable components of software hardware and the migration of VLSI design to high level synthesis based on HDLs Currently the subject has reached the consolidation phase in which languages and standards are being increasingly used at the same time as the scope is being broadened to additional application areas This book presents the latest developments in this area and provides a forum from which readers can learn from the past and look forward to what the future holds

Electronic Design Automation for IC System Design, Verification, and Testing

Luciano Lavagno, Igor L. Markov, Grant Martin, Louis K. Scheffer, 2017-12-19 The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logic verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for integrated circuit IC designs design and verification languages digital simulation hardware acceleration and emulation and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on high level synthesis system on chip SoC block based design and back annotating system level models Offering improved depth and modernity Electronic Design Automation for IC System Design Verification and Testing provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals

International Symposium on Quality Electronic Design , 2002 Annotation Fifty one papers and 21 posters from the March 2002 symposium report current research in deep submicron integrated circuit design and development The sessions address interconnect extraction and modeling design for process variations metrics power and noise management verification signal

integrity and low power design techniques Some of the topics are transition aware global signaling TAGS the interoperability of EDA tools for sequential logic synthesis statistical methods for the determination of process corners power supply noise suppression via clock skew scheduling and the relation between SAT and BDDs for equivalence checking No subject index Annotation copyrighted by Book News Inc Portland OR *Hardware/Software Co-Design* Jørgen Staunstrup, Wayne Wolf, 2013-04-17 Introduction to Hardware Software Co Design presents a number of issues of fundamental importance for the design of integrated hardware software products such as embedded communication and multimedia systems This book is a comprehensive introduction to the fundamentals of hardware software co design Co design is still a new field but one which has substantially matured over the past few years This book written by leading international experts covers all the major topics including fundamental issues in co design hardware software co synthesis algorithms prototyping and emulation target architectures compiler techniques specification and verification system level specification Special chapters describe in detail several leading edge co design systems including Cosyma LYCOS and Cosmos Introduction to Hardware Software Co Design contains sufficient material for use by teachers and students in an advanced course of hardware software co design It also contains extensive explanation of the fundamental concepts of the subject and the necessary background to bring practitioners up to date on this increasingly important topic *Introduction to Logic Circuits & Logic Design with VHDL* Brock J. LaMeres, 2019-03-19 This textbook introduces readers to the fundamental hardware used in modern computers The only pre requisite is algebra so it can be taken by college freshman or sophomore students or even used in Advanced Placement courses in high school This book presents both the classical approach to digital system design i e pen and paper in addition to the modern hardware description language HDL design approach computer based This textbook enables readers to design digital systems using the modern HDL approach while ensuring they have a solid foundation of knowledge of the underlying hardware and theory of their designs This book is designed to match the way the material is actually taught in the classroom Topics are presented in a manner which builds foundational knowledge before moving onto advanced topics The author has designed the content with learning goals and assessment at its core Each section addresses a specific learning outcome that the learner should be able to do after its completion The concept checks and exercise problems provide a rich set of assessment tools to measure learner performance on each outcome This book can be used for either a sequence of two courses consisting of an introduction to logic circuits Chapters 1 7 followed by logic design Chapters 8 13 or a single accelerated course that uses the early chapters as reference material *Principles of Verifiable RTL Design* Lionel Bening, Harry D. Foster, 2007-05-08 Principles of Verifiable RTL Design A Functional Coding Style Supporting Verification Processes in Verilog explains how you can write Verilog to describe chip designs at the RT level in a manner that cooperates with verification processes This cooperation can return an order of magnitude improvement in performance and capacity from tools such as simulation and equivalence checkers It reduces the labor costs of coverage and formal model checking by

facilitating communication between the design engineer and the verification engineer It also orients the RTL style to provide more useful results from the overall verification process The intended audience for Principles of Verifiable RTL Design A Functional Coding Style Supporting Verification Processes in Verilog is engineers and students who need an introduction to various design verification processes and a supporting functional Verilog RTL coding style A second intended audience is engineers who have been through introductory training in Verilog and now want to develop good RTL writing practices for verification A third audience is Verilog language instructors who are using a general text on Verilog as the course textbook but want to enrich their lectures with an emphasis on verification A fourth audience is engineers with substantial Verilog experience who want to improve their Verilog practice to work better with RTL Verilog verification tools A fifth audience is design consultants searching for proven verification centric methodologies A sixth audience is EDA verification tool implementers who want some suggestions about a minimal Verilog verification subset Principles of Verifiable RTL Design A Functional Coding Style Supporting Verification Processes in Verilog is based on the reality that comes from actual large scale product design process and tool experience

Encyclopedia of Microcomputers Allen Kent,James G. Williams,2000-06-30 This encyclopaedia covers An Algorithm for Abductive Inference in Artificial Intelligence to Web Financial Information System Server

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