

Advanced Hardware Design and Petri nets

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Hardware Design And Petri Nets

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Hardware Design And Petri Nets:

Hardware Design and Petri Nets Alex Yakovlev, Luis Gomes, Luciano Lavagno, 2013-04-17 Hardware Design and Petri Nets presents a summary of the state of the art in the applications of Petri nets to designing digital systems and circuits The area of hardware design has traditionally been a fertile field for research in concurrency and Petri nets Many new ideas about modelling and analysis of concurrent systems and Petri nets in particular originated in theory of asynchronous digital circuits Similarly the theory and practice of digital circuit design have always recognized Petri nets as a powerful and easy to understand modelling tool The ever growing demand in the electronic industry for design automation to build various types of computer based systems creates many opportunities for Petri nets to establish their role of a formal backbone in future tools for constructing systems that are increasingly becoming distributed concurrent and asynchronous Petri nets have already proved very effective in supporting algorithms for solving key problems in synthesis of hardware control circuits However since the front end to any realistic design flow in the future is likely to rely on more pragmatic Hardware Description Languages HDLs such as VHDL and Verilog it is crucial that Petri nets are well interfaced to such languages Hardware Design and Petri Nets is divided into five parts which cover aspects of behavioral modelling analysis and verification synthesis from Petri nets and STGs design environments based on high level Petri nets and HDLs and finally performance analysis using Petri nets Hardware Design and Petri Nets serves as an excellent reference source and may be used as a text for advanced courses on the subject

Hardware Design and Petri Nets Alex Yakovlev, Luis Gomes, Luciano Lavagno, 2014-01-15

Concurrency and Hardware Design Jordi Cortadella, Alex Yakovlev, Grzegorz Rozenberg, 2003-07-01 As CMOS semiconductor technology strides towards billions of transistors on a single die new problems arise on the way They are concerned with the minishing fabrication process features which a ect for example the gate to wire delay ratio They manifest themselves in greater variations of size and operating parameters of devices which put the overall reliability of systems at risk And most of all they have tremendous impact on design productivity where the costs of utilizing the growing silicon real estate rocket to billions of dollars that have to be spent on design veri cation and testing All such problems call for new sign approaches and models for digital systems Furthermore new developments in non CMOS technologies such as single electron transistors rapid single quantum devices quantum dot cells molecular devices etc add extra demand for new research in system design methodologies What kind of models and design methodologies will be required to build systems in all these new technologies Answering this question even for each particular type of new technology generation is not easy especially because sometimes it is not even clear what kind of elementary devices are feasible there This problem is of an interdisciplinary nature It requires an bridges between di erent scienti c communities The bridges must be built very quickly and be maximally exible to accommodate changes taking place in a logarithmic timescale

Concurrency and Hardware Design Jordi Cortadella, Alex Yakovlev, Grzegorz Rozenberg, 2002-11-26 As CMOS semiconductor technology strides towards

billions of transistors on a single die new problems arise on the way They are concerned with the minishing fabrication process features which a ect for example the gate to wire delay ratio They manifest themselves in greater variations of size and operating parameters of devices which put the overall reliability of systems at risk And most of all they have tremendous impact on design productivity where the costs of utilizing the growing silicon real estate rocket to billions of dollars that have to be spent on design veri cation and testing All such problems call for new sign approaches and models for digital systems Furthermore new developments in non CMOS technologies such as single electron transistors rapid single quantum devices quantum dot cells molecular devices etc add extra demand for new research in system design methodologies What kind of models and design methodologies will be required to build systems in all these new technologies Answering this question even for each particular type of new technology generation is not easy especially because sometimes it is not even clear what kind of elementary devices are feasible there This problem is of an interdisciplinary nature It requires an bridges between di erent scienti c communities The bridges must be built very quickly and be maximally exible to accommodate changes taking place in a logarithmic timescale

Lectures on Petri Nets II: Applications Wolfgang Reisig,Grzegorz Rozenberg,1998-11-04 The two volume set originates from the Advanced Course on Petri Nets held in Dagstuhl Germany in September 1996 beyond the lectures given there additional chapters have been commissioned to give a well balanced presentation of the state of the art in the area Together with its companion volume *Lectures on Petri Nets I Basic Models* this book is the actual reference for the area and addresses professionals students lecturers and researchers who are interested in systems design and would like to learn to use Petri nets familiar with subareas of the theory or its applications and wish to view the whole area interested in learning about recent results presented within a unified framework planning to apply Petri nets in practical situations interested in the relationship of Petri nets to other models of concurrent systems

Practical Formal Methods for Hardware Design Carlos Delgado Kloos,Werner Damm,2012-12-06 Formal methods for hardware design still find limited use in industry Yet current practice has to change to cope with decreasing design times and increasing quality requirements This research report presents results from the Esprit project FORMAT formal methods in hardware verification which involved the collaboration of the enterprises Siemens Italtel Telefonica I D TGI and AHL the research institute OFFIS and the universities of Madrid and Passau The work presented involves advanced specification languages for hardware design that are intuitive to the designer like timing diagrams and state based languages as well as their relation to VHDL and formal languages like temporal logic and a process algebraic calculus The results of experimental tests of the tools are also presented

Correct Hardware Design and Verification Methods Tiziana Margaria,Tom F. Melham,2001-08-27 This book constitutes the refereed proceedings of the 11th IFIP WG 10 5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods CHARME 2001 held in Livingston Scotland UK in September 2001 The 28 revised full papers and eight short papers presented together with two invited papers and one special paper were carefully reviewed and selected from 56

submissions The book offers topical sections on model checking clocking issues theorem proving with higher order logics hardware compilation tools component verification case studies algorithm verification and duration calculus

Application and Theory of Petri Nets 1993 Marco Ajmone Marsan,1993-06-07 This volume contains the proceedings of the 14th International Conference on Application and Theory of Petri Nets The aim of the Petri net conferences is to create a forum for discussing progress in the application and theory of Petri nets Typically the conferences have 150 200 participants one third of whom come from industry while the rest are from universities and research institutes The volume includes three invited papers Modeling and enactment of workflow systems C A Ellis G J Nutt Interleaving functional and performance structural analysis of net models M Silva and FSPNs fluid stochastic Petri nets K S Trivedi V G Kulkarni together with 26 full papers selected from 102 submissions and 6 project papers

Correct Hardware Design and Verification Methods George J. Milne, Laurence Pierre,1993-05-12 These proceedings contain the papers presented at the Advanced Research Working Conference on Correct Hardware Design Methodologies held in Arles France in May 1993 and organized by the ESPRIT Working Group 6018 CHARME 2 and the Universit de Provence Marseille in cooperation with IFIP Working Group 10 2 Formal verification is emerging as a plausible alternative to exhaustive simulation for establishing correct digital hardware designs The validation of functional and timing behavior is a major bottleneck in current VLSI design systems slowing the arrival of products in the marketplace with its associated increase in cost From being a predominantly academic area of study until a few years ago formal design and verification techniques are now beginning to migrate into industrial use As we are now witnessing an increase in activity in this area in both academia and industry the aim of this working conference was to bring together researchers and users from both communities

Handbook of Research on Discrete Event Simulation Environments: Technologies and Applications Abu-Taieh, Evon M. O., El-Sheikh, Asim A.,2009-10-31 This book provides a comprehensive overview of theory and practice in simulation systems focusing on major breakthroughs within the technological arena with particular concentration on the accelerating principles concepts and applications Provided by publisher

Prototyping of Concurrent Control Systems Implemented in FPGA Devices Remigiusz Wiśniewski,2016-09-30 This book focuses on prototyping aspects of concurrent control systems and their further implementation and partial reconfiguration in programmable devices Further it lays out a full prototyping flow for concurrent control systems Based on a given primary specification a system is described with an interpreted Petri net which naturally reflects the concurrent and sequential relationships of the design The book shows that apart from the traditional option of static configuration of the entire system the latest programmable devices especially FPGAs offer far more sophistication Partial reconfiguration allows selected parts of the system to be replaced without having to reprogram the entire structure of the device Approaches to dynamic and static partial reconfiguration of concurrent control systems are presented and described in detail p The theoretical work is illustrated by examples drawn from various applications with a milling machine and a traffic light

controller highlighted as representative interpreted Petri nets Given the ubiquity of concurrent control systems in a huge variety of technological areas including transportation medicine artificial intelligence manufacturing security and safety and planetary exploration the innovative software and hardware design methods described here will be of considerable interest to control engineers and systems and circuits researchers in many areas of industry and academia Readings in

Hardware/Software Co-Design Giovanni De Micheli,Rolf Ernst,Wayne Wolf,2002 This title serves as an introduction and reference for the field with the papers that have shaped the hardware software co design since its inception in the early 90s

Hardware/Software Co-Design Giovanni DeMicheli,M.G. Sami,2013-11-11 Concurrent design or co design of hardware and software is extremely important for meeting design goals such as high performance that are the key to commercial competitiveness Hardware Software Co Design covers many aspects of the subject including methods and examples for designing 1 general purpose and embedded computing systems based on instruction set processors 2 telecommunication systems using general purpose digital signal processors as well as application specific instruction set processors 3 embedded control systems and applications to automotive electronics The book also surveys the areas of emulation and prototyping systems with field programmable gate array technologies hardware software synthesis and verification and industrial design trends Most contributions emphasize the design methodology the requirements and state of the art of computer aided co design tools together with current design examples **Multimedia and Ubiquitous Engineering** James J. (Jong Hyuk)

Park,Shu-Ching Chen,Joon-Min Gil,Neil Y. Yen,2014-04-16 The aims of these proceedings are to provide a complete coverage of the areas outlined and to bring together researchers from academic and industry to share ideas challenges and solutions relating to the multifaceted aspects of this field New multimedia standards for example MPEG 21 facilitate the seamless integration of multiple modalities into interoperable multimedia frameworks transforming the way people work and interact with multimedia data These key technologies and multimedia solutions interact and collaborate with each other in increasingly effective ways contributing to the multimedia revolution and having a significant impact across a wide spectrum of consumer business healthcare education and governmental domains **STG Decomposition: Internal Communication**

for SI Implementability Dominic Wist,Mark Schaefer,Walter Vogler,Ralf Wollowski,2010 STG decomposition is a promising approach to tackle the complexity problems arising in logic synthesis of speed independent circuits a robust asynchronous i e clockless circuit type Unfortunately STG decomposition can result in components that in isolation have irreducible CSC conflicts Generalising earlier work it is shown how to resolve such conflicts by introducing internal communication between the components via structural techniques only Technological Innovation for Digitalization and Virtualization Luis M. Camarinha-Matos,2022-06-21 This book constitutes the refereed proceedings of the 13th IFIP WG 5.5 SOCOLNET Advanced Doctoral Conference on Computing Electrical and Industrial Systems DoCEIS 2022 held in Caparica Portugal during June July 2022 The 22 full papers presented were carefully reviewed and selected from 48 submissions The papers present

selected results produced in engineering doctoral programs and focus on technological innovation for industry and service systems The papers are organized into the following topical sub headings Smart Systems Thinking Cyber physical Systems health related Digitalization Electric Systems and Machines Smart Devices and Control and Digital Platforms *Computer Hardware Description Languages and their Applications* D. Borriane,R. Waxman,2014-06-28 The topic areas presented within this volume focus on design environments and the applications of hardware description and modelling including simulation verification by correctness proofs synthesis and test The strong relationship between the topics of CHDL 91 and the work around the use and re standardization of the VHDL language is also explored The quality of this proceedings and its significance to the academic and professional worlds is assured by the excellent technical programme here compiled

Multiprocessor Systems-on-Chips Ahmed Jerraya,Wayne Wolf,2005 Modern system on chip SoC design shows a clear trend toward integration of multiple processor cores on a single chip Designing a multiprocessor system on chip MPSOC requires an understanding of the various design styles and techniques used in the multiprocessor Understanding the application area of the MPSOC is also critical to making proper tradeoffs and design decisions Multiprocessor Systems on Chips covers both design techniques and applications for MPSOCs Design topics include multiprocessor architectures processors operating systems compilers methodologies and synthesis algorithms and application areas covered include telecommunications and multimedia The majority of the chapters were collected from presentations made at the International Workshop on Application Specific Multi Processor SoC held over the past two years The workshop assembled internationally recognized speakers on the range of topics relevant to MPSOCs After having refined their material at the workshop the speakers are now writing chapters and the editors are fashioning them into a unified book by making connections between chapters and developing common terminology Examines several different architectures and the constraints imposed on them Discusses scheduling real time operating systems and compilers Analyzes design trade off and decisions in telecommunications and multimedia applications **A Designer's Guide to Asynchronous VLSI** Peter A. Beerel,Recep O. Ozdag,Marcos Ferretti,2010-02-04 Create low power higher performance circuits with shorter design times using this practical guide to asynchronous design This practical alternative to conventional synchronous design enables performance close to full custom designs with design times that approach commercially available ASIC standard cell flows It includes design trade offs specific design examples and end of chapter exercises Emphasis throughout is placed on practical techniques and real world applications making this ideal for circuit design students interested in alternative design styles and system on chip circuits as well as circuit designers in industry who need new solutions to old problems Hardware Description Languages and their Applications Carlos Delgado Kloos,Eduard Cerny,2013-06-05 In the past few decades Computer Hardware Description Languages CHDLs have been a rapidly expanding subject area due to a number of factors including the advancing complexity of digital electronics the increasing prevalence of generic and programmable

components of software hardware and the migration of VLSI design to high level synthesis based on HDLs. Currently the subject has reached the consolidation phase in which languages and standards are being increasingly used at the same time as the scope is being broadened to additional application areas. This book presents the latest developments in this area and provides a forum from which readers can learn from the past and look forward to what the future holds.

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