

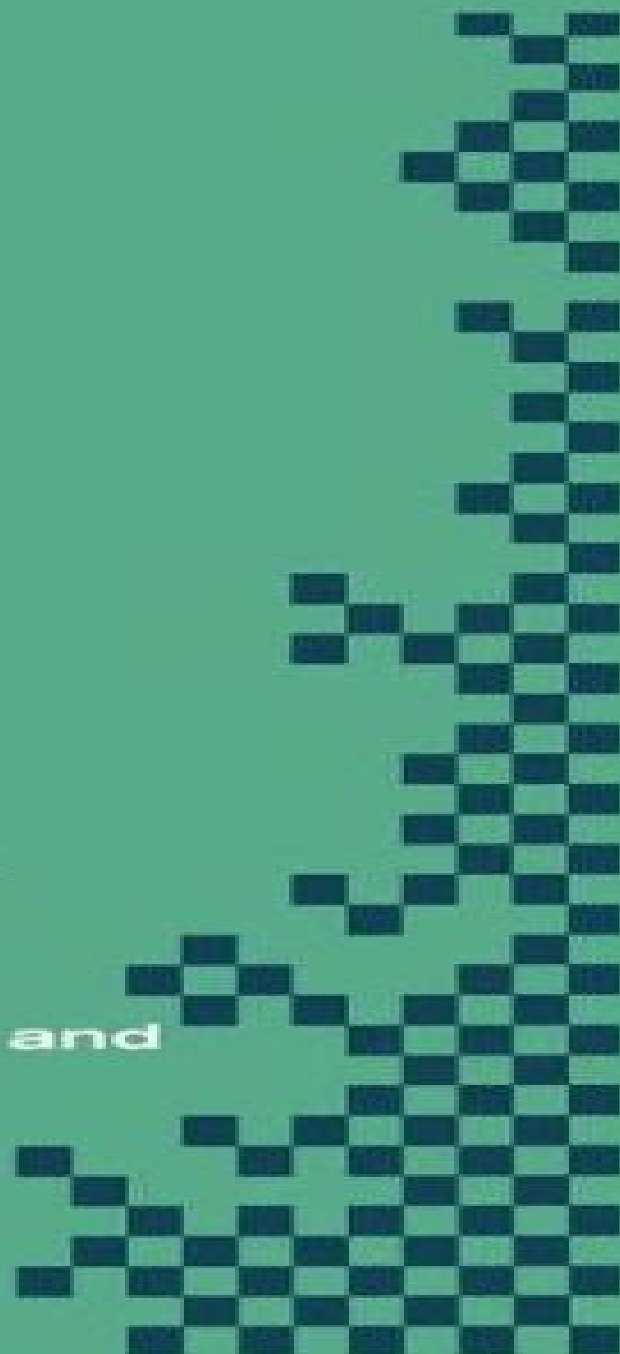
Hardware Description Languages and their Applications

Specification, modelling,
verification and synthesis
of microelectronic systems

Edited by
**Carlos Delgado Kloos and
Eduard Cerny**



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Hardware Description Languages And Their Applications Specification Modelling Verification And Synthesis

Anupam Chattopadhyay



Hardware Description Languages And Their Applications Specification Modelling Verification And Synthesis:

Hardware Description Languages and their Applications Carlos Delgado Kloos, Eduard Cerny, 2013-06-05 In the past few decades Computer Hardware Description Languages CHDLs have been a rapidly expanding subject area due to a number of factors including the advancing complexity of digital electronics the increasing prevalence of generic and programmable components of software hardware and the migration of VLSI design to high level synthesis based on HDLs Currently the subject has reached the consolidation phase in which languages and standards are being increasingly used at the same time as the scope is being broadened to additional application areas This book presents the latest developments in this area and provides a forum from which readers can learn from the past and look forward to what the future holds

Computer Hardware Description Languages and their Applications D. Borriore, R. Waxman, 2014-06-28 The topic areas presented within this volume focus on design environments and the applications of hardware description and modelling including simulation verification by correctness proofs synthesis and test The strong relationship between the topics of CHDL 91 and the work around the use and re standardization of the VHDL language is also explored The quality of this proceedings and its significance to the academic and professional worlds is assured by the excellent technical programme here compiled

Computer Hardware Description Languages and their Applications D. Agnew, L. Claesen, R. Camposano, 2014-05-21 Hardware description languages HDLs have established themselves as one of the principal means of designing electronic systems The interest in and usage of HDLs continues to spread rapidly driven by the increasing complexity of systems the growth of HDL driven synthesis the research on formal design methods and many other related advances This research oriented publication aims to make a strong contribution to further developments in the field The following topics are explored in depth BDD based system design and analysis system level formal verification formal reasoning on hardware languages for protocol specification VHDL HDL based design methods high level synthesis and text graphical HDLs There are short papers covering advanced design capture and recent work in high level synthesis and formal verification In addition several invited presentations on key issues discuss and summarize recent advances in real time system design automatic verification of sequential circuits and languages for protocol specification

Advanced VLSI Design and Testability Issues Suman Lata Tripathi, Sobhit Saxena, Sushanta Kumar Mohapatra, 2020-08-19 This book facilitates the VLSI interested individuals with not only in depth knowledge but also the broad aspects of it by explaining its applications in different fields including image processing and biomedical The deep understanding of basic concepts gives you the power to develop a new application aspect which is very well taken care of in this book by using simple language in explaining the concepts In the VLSI world the importance of hardware description languages cannot be ignored as the designing of such dense and complex circuits is not possible without them Both Verilog and VHDL languages are used here for designing The current needs of high performance integrated circuits ICs including low power devices and new emerging materials which can play a very important role in

achieving new functionalities are the most interesting part of the book. The testing of VLSI circuits becomes more crucial than the designing of the circuits in this nanometer technology era. The role of fault simulation algorithms is very well explained and its implementation using Verilog is the key aspect of this book. This book is well organized into 20 chapters. Chapter 1 emphasizes on uses of FPGA on various image processing and biomedical applications. Then the descriptions enlighten the basic understanding of digital design from the perspective of HDL in Chapters 2-5. The performance enhancement with alternate material or geometry for silicon based FET designs is focused in Chapters 6 and 7. Chapters 8 and 9 describe the study of bimolecular interactions with biosensing FETs. Chapters 10-13 deal with advanced FET structures available in various shapes/materials such as nanowire HFET and their comparison in terms of device performance metrics calculation. Chapters 14-18 describe different application specific VLSI design techniques and challenges for analog and digital circuit designs. Chapter 19 explains the VLSI testability issues with the description of simulation and its categorization into logic and fault simulation for test pattern generation using Verilog HDL. Chapter 20 deals with a secured VLSI design with hardware obfuscation by hiding the IC's structure and function which makes it much more difficult to reverse engineer.

Architecture and Design of Distributed Embedded Systems Bernd Kleinjohann, 2013-04-18. Due to the decreasing production costs of IT systems, applications that had to be realised as expensive PCBs formerly can now be realised as a system on chip. Furthermore, low cost broadband communication media for wide area communication as well as for the realisation of local distributed systems are available. Typically, the market requires IT systems that realise a set of specific features for the end user in a given environment, so called embedded systems. Some examples for such embedded systems are control systems in cars, airplanes, houses or plants, information and communication devices like digital TV, mobile phones or autonomous systems like service or edutainment robots. For the design of embedded systems, the designer has to tackle three major aspects: The application itself including the man-machine interface, the target architecture of the system including all functional and non-functional constraints, and the design methodology including modelling, specification, synthesis, test and validation. The last two points are a major focus of this book. This book documents the high quality approaches and results that were presented at the International Workshop on Distributed and Parallel Embedded Systems (DIPES 2000) which was sponsored by the International Federation for Information Processing (IFIP) and organised by IFIP working groups WG10.3, WG10.4 and WG10.5. The workshop took place on October 18-19, 2000 in Schlo Eringerfeld near Paderborn, Germany. Architecture and Design of Distributed Embedded Systems is organised similar to the workshop. Chapters 1 and 4 (Methodology I and II) deal with different modelling and specification paradigms and the corresponding design methodologies. Generic system architectures for different classes of embedded systems are presented in Chapter 2. In Chapter 3, several design environments for the support of specific design methodologies are presented. Problems concerning test and validation are discussed in Chapter 5. The last two chapters include distribution and communication aspects. Chapter 6 and synthesis

techniques for embedded systems Chapter 7 This book is essential reading for computer science researchers and application developers **NASA Formal Methods** Mihaela Bobaru,Klaus Havelund,Gerard Holzmann,Rajeev Joshi,2011-04-06 This book constitutes the refereed proceedings of the Third International Symposium on NASA Formal Methods NFM 2011 held in Pasadena CA USA in April 2011 The 26 revised full papers presented together with 12 tool papers 3 invited talks and 2 invited tutorials were carefully reviewed and selected from 141 submissions The topics covered by NFM 2011 included but were not limited to theorem proving logic model checking automated testing and simulation model based engineering real time and stochastic systems SAT and SMT solvers symbolic execution abstraction and abstraction refinement compositional verification techniques static and dynamic analysis techniques fault protection cyber security specification formalisms requirements analysis and applications of formal techniques **Readings in Hardware/Software Co-Design** Giovanni De Micheli,Rolf Ernst,Wayne Wolf,2002 This title serves as an introduction and reference for the field with the papers that have shaped the hardware software co design since its inception in the early 90s *Fundamentals and Standards in Hardware Description Languages* Jean Mermet,2012-12-06 The second half of this century will remain as the era of proliferation of electronic computers They did exist before but they were mechanical During next century they may perform other mutations to become optical or molecular or even biological Actually all these aspects are only fancy dresses put on mathematical machines This was always recognized to be true in the domain of software where machine or high level languages are more or less rigorous but immaterial variations of the universally accepted mathematical language aimed at specifying elementary operations functions algorithms and processes But even a mathematical machine needs a physical support and this is what hardware is all about The invention of hardware description languages HDL s in the early 60 s was an attempt to stay longer at an abstract level in the design process and to push the stage of physical implementation up to the moment when no more technology independent decisions can be taken It was also an answer to the continuous exponential growth of complexity of systems to be designed This problem is common to hardware and software and may explain why the syntax of hardware description languages has followed with a reasonable delay of ten years the evolution of the programming languages at the end of the 60 s they were Algol like a decade later Pascal like and now they are C or ADA like They have also integrated the new concepts of advanced software specification languages *Mechatronic Systems* Georg Pelz,2003-06-02 Covers the modelling and simulation of mechatronic and micromechatronic systems using HDLs Provides an overview of the design of digital and analog circuitry and software for mechatronic systems Presents practical guidance on both chip and systems design for a wide range of mechatronic applications Focuses on a practical approach to the design and simulation of electronic hardware and components of mechatronic systems **Optimized ASIP Synthesis from Architecture Description Language Models** Oliver Schliebusch,Heinrich Meyr,Rainer Leupers,2007-04-27 New software tools and a sophisticated methodology above RTL are required to answer the challenges of designing an optimized application specific

processor ASIP This book offers an automated and fully integrated implementation flow and compares it to common implementation practice Case studies emphasise that neither the architectural advantages nor the design space of ASIPs are sacrificed for an automated implementation Realizing a building block which fulfils the requirements on programmability and computational power is now efficiently possible for the first time Optimized ASIP Synthesis from Architecture Description Language Models inspires hardware designers as well as application engineers to design powerful ASIPs that will make their SoC designs unique

Computer Hardware Description Languages and Their Applications John A. Darringer, F. J. Rammig, 1990 Languages for precisely describing the behavior of computers have been studied since the conception of the computer itself As the computer industry has grown so has the need to exchange information about computers Computer Hardware Description Languages CHDL are required to provide specifications and detailed implementation for a growing menu of sophisticated design automation tools including synthesis verification simulation analysis optimization placement wiring and testing communicate requirements and capabilities between suppliers and users of computer components and subsystems facilitate the transfer of new methods and results within the university and industrial research community As reflected in this book there is an increased emphasis on applications and resulting requirements that are placed on CHDLs In the field of synthesis a major application area there is today a focus on high level synthesis and synthesis under design constraints In the area of design correctness research has shifted away from simulation to formal verification techniques such as temporal logic

Theorem Provers in Circuit Design Ramayya Kumar, Thomas Kropf, 1995-03-06 This two volume set contains papers presented at the International Conference on Computational Engineering Science ICES 95 held in Mauna Lani Hawaii from 30 July to 3 August 1995 The contributions capture the state of the science in computational modeling and simulation in a variety of engineering disciplines civil mechanical aerospace materials and electronics engineering

Correct Hardware Design and Verification Methods George J. Milne, Laurence Pierre, 1993-05-12 These proceedings contain the papers presented at the Advanced Research Working Conference on Correct Hardware Design Methodologies held in Arles France in May 1993 and organized by the ESPRIT Working Group 6018 CHARME 2 and the Universit de Provence Marseille in cooperation with IFIP Working Group 10.2 Formal verification is emerging as a plausible alternative to exhaustive simulation for establishing correct digital hardware designs The validation of functional and timing behavior is a major bottleneck in current VLSI design systems slowing the arrival of products in the marketplace with its associated increase in cost From being a predominantly academic area of study until a few years ago formal design and verification techniques are now beginning to migrate into industrial use As we are now witnessing an increase in activity in this area in both academia and industry the aim of this working conference was to bring together researchers and users from both communities

Practical Formal Methods for Hardware Design Carlos Delgado Kloos, Werner Damm, 2012-12-06 Formal methods for hardware design still find limited use in industry Yet current practice has to change to cope with

decreasing design times and increasing quality requirements This research report presents results from the Esprit project FORMAT formal methods in hardware verification which involved the collaboration of the enterprises Siemens Italtel Telefonica I D TGI and AHL the research institute OFFIS and the universities of Madrid and Passau The work presented involves advanced specification languages for hardware design that are intuitive to the designer like timing diagrams and state based languages as well as their relation to VHDL and formal languages like temporal logic and a process algebraic calculus The results of experimental tests of the tools are also presented Handbook of Computer Architecture Anupam Chattopadhyay,2024-12-20 This handbook presents the key topics in the area of computer architecture covering from the basic to the most advanced topics including software and hardware design methodologies It will provide readers with the most comprehensive updated reference information covering applications in single core processors multicore processors application specific processors reconfigurable architectures emerging computing architectures processor design and programming flows test and verification This information benefits the readers as a full and quick technical reference with a high level review of computer architecture technology detailed technical descriptions and the latest practical applications

Models, Methods, and Tools for Complex Chip Design Jan Haase,2013-09-18 This book brings together a selection of the best papers from the fifteenth edition of the Forum on specification and Design Languages Conference FDL which was held in September 2012 at Vienna University of Technology Vienna Austria FDL is a well established international forum devoted to dissemination of research results practical experiences and new ideas in the application of specification design and verification languages to the design modeling and verification of integrated circuits complex hardware software embedded systems and mixed technology systems **System-on-Chip for Real-Time Applications** Wael Badawy,Graham A. Julien,2012-12-06 System on Chip for Real Time Applications will be of interest to engineers both in industry and academia working in the area of SoC VLSI design and application It will also be useful to graduate and undergraduate students in electrical and computer engineering and computer science A selected set of papers from the 2nd International Workshop on Real Time Applications were used to form the basis of this book It is organized into the following chapters Introduction Design Reuse Modeling Architecture Design Techniques Memory Circuits Low Power Interconnect and Technology MEMS System on Chip for Real Time Applications contains many signal processing applications and will be of particular interest to those working in that community Computer-Aided Verification Robert Kurshan,2012-12-06 Computer Aided Verification is a collection of papers that begins with a general survey of hardware verification methods Ms Gupta starts with the issue of verification itself and develops a taxonomy of verification methodologies focusing especially upon recent advances Although her emphasis is hardware verification most of what she reports applies to software verification as well Graphical presentation is coming to be a de facto requirement for a friendly user interface The second paper presents a generic format for graphical presentations of coordinating systems represented by automata The last two papers as a pair present a variety of generic

techniques for reducing the computational cost of computer aided verification based upon explicit computational memory the first of the two gives a time space trade off while the second gives a technique which trades space for a sometimes predictable probability of error Computer Aided Verification is an edited volume of original research This research work has also been published as a special issue of the journal Formal Methods in System Design 1 2 3 **Embedded Systems Handbook** Richard Zurawski, 2018-09-03 Considered a standard industry resource the Embedded Systems Handbook provided researchers and technicians with the authoritative information needed to launch a wealth of diverse applications including those in automotive electronics industrial automated systems and building automation and control Now a new resource is required to report on current developments and provide a technical reference for those looking to move the field forward yet again Divided into two volumes to accommodate this growth the Embedded Systems Handbook Second Edition presents a comprehensive view on this area of computer engineering with a currently appropriate emphasis on developments in networking and applications Those experts directly involved in the creation and evolution of the ideas and technologies presented offer tutorials research surveys and technology overviews that explore cutting edge developments and deployments and identify potential trends This first self contained volume of the handbook Embedded Systems Design and Verification is divided into three sections It begins with a brief introduction to embedded systems design and verification It then provides a comprehensive overview of embedded processors and various aspects of system on chip and FPGA as well as solutions to design challenges The final section explores power aware embedded computing design issues specific to secure embedded systems and web services for embedded devices Those interested in taking their work with embedded systems to the network level should complete their study with the second volume Network Embedded Systems [VHDL User's Forum in Europe](#) Eugenio Villar Bonet, 1997 Compendio de los trabajos presentados en Toledo durante el VHDL user s forum in Europe

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